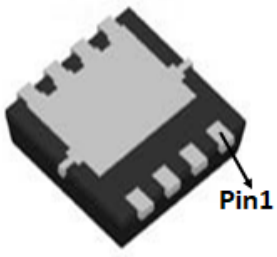
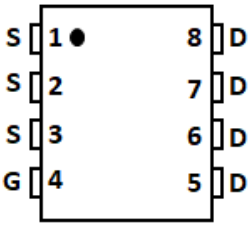
Leiditech

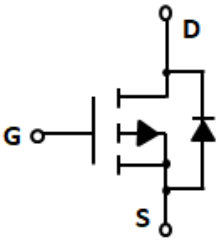
LMQ40P03A

P-Channel Enhancement Mode Field Effect Transistor





DFN3.3X3.3



Product Summary

- V_{DS} -30V
- I_D -40A
- $R_{DS(ON)}$(at V_{GS}=-20V) ＜13 mohm
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜15 mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜25 mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery management
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	±25	V
Drain Current	T_A=25℃ @ Steady State	I_D	-40	A
	T_A=70℃ @ Steady State		-33	
Pulsed Drain Current [A]		I_{DM}	-160	A
Single Pulse Avalanche Energy @L=0.5mH [B]		E_{AS}	72	mJ
Total Power Dissipation @ T_A=25℃ [C]		P_D	32	W
Thermal Resistance Junction-to-Ambient @ Steady State [D]		$R_{\theta JA}$	4.0	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
LMQ40P03A	F1	Q40P03	5000			13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±25V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -20V, I_D=-20A		8.6	13	mΩ
		V_{GS}= -10V, I_D=-15A		9.8	15	
		V_{GS}= -6.0V, I_D=-12A		12.1	22	
		V_{GS}= -4.5V, I_D=-12A		15.5	25	
Diode Forward Voltage	V_{SD}	I_S=-20A,V_{GS}=0V			-1.2	V
Maximum Body-Diode Continuous Current	I_S				-40	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ		2050		pF
Output Capacitance	C_{oss}			355		
Reverse Transfer Capacitance	C_{rss}			301		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-20A		29.8		nC
Gate Source Charge	Q_{gs}			4.7		
Gate Drain Charge	Q_{gd}			10		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-15V, I_D=-1A, R_{GEN}=2.5Ω		14		ns
Turn-on Rise Time	t_r			12		
Turn-off Delay Time	$t_{D(off)}$			26		
Turn-off Fall Time	t_f			10		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep Initial T_J=25℃.

C. The power dissipation PD is based on $T_{J(MAX)}$=150℃, using ≤ 10s junction-to-ambient thermal resistance.

D. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25℃. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

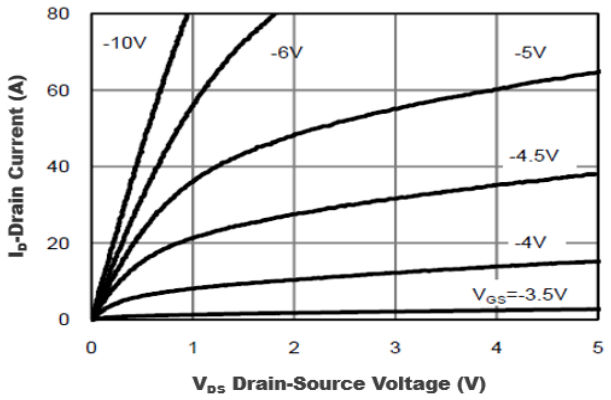


Figure1. Output Characteristics

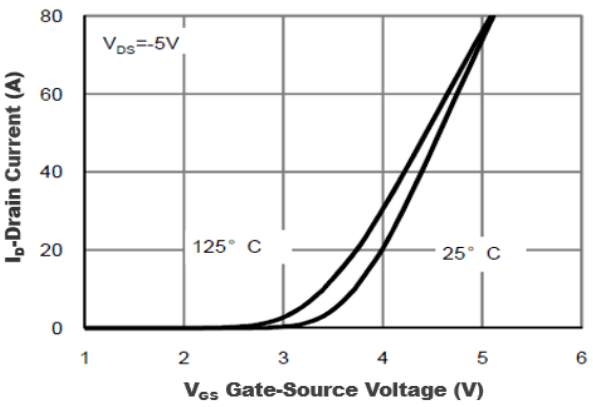


Figure2. Transfer Characteristics

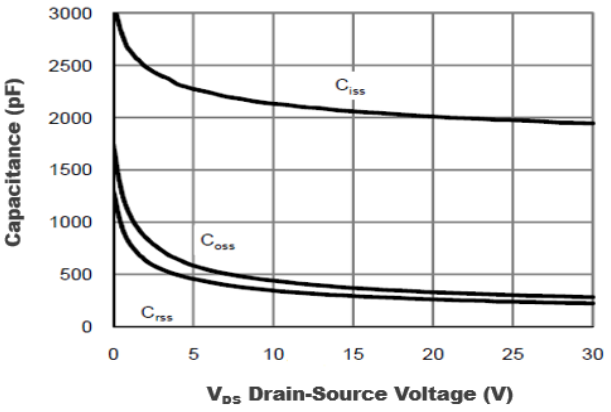


Figure3. Capacitance Characteristics

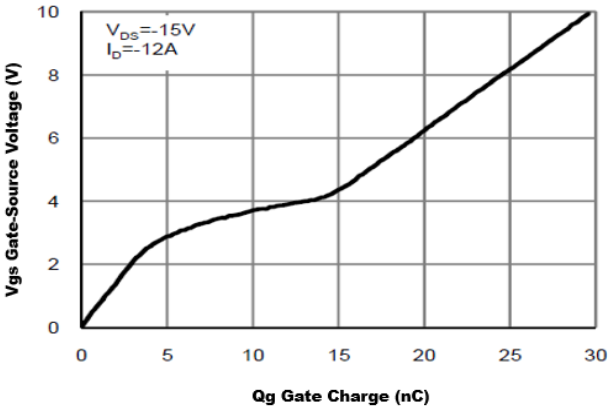


Figure4. Gate Charge

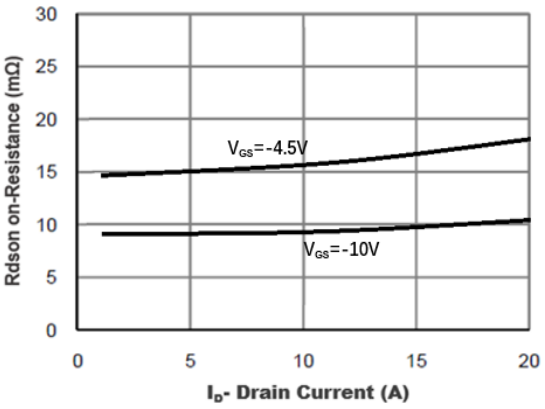


Figure5. Drain-Source on Resistance

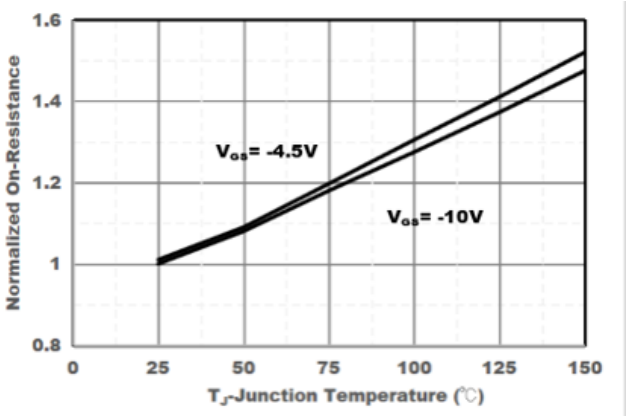


Figure6. Drain-Source on Resistance

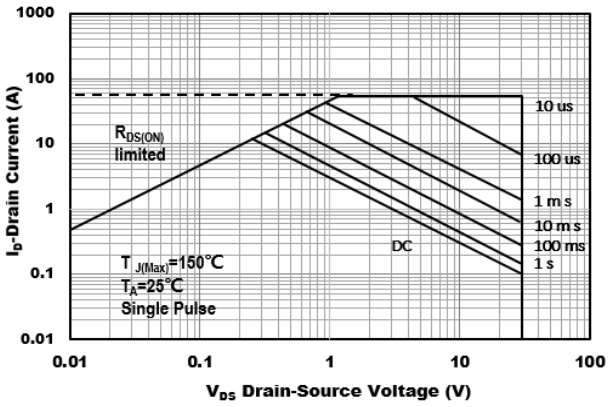


Figure7. Safe Operation Area

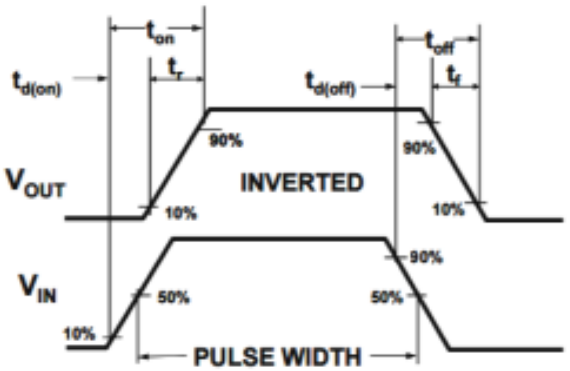
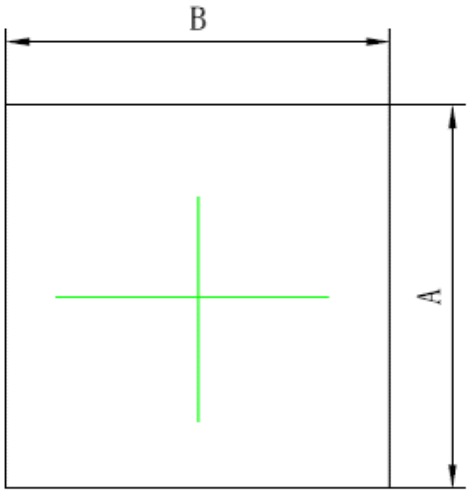
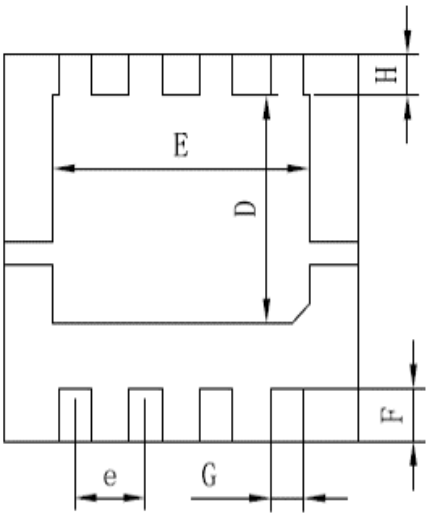
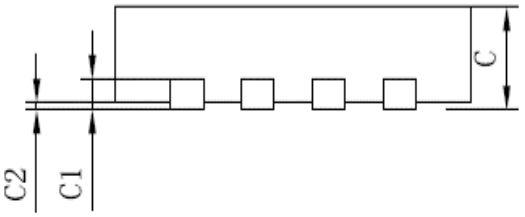


Figure8. Switching wave

■ DFN3.3×3.3 Package information







A	B	C	C1
3.25±0.05	3.25±0.05	0.8±0.05	0.2±0.02
C2	D	E	F
0.05Max	1.9±0.1	2.35±0.15	0.45±0.05
G	H	e	
0.3±0.05	0.35±0.05	0.65±0.05	
单位：mm			

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