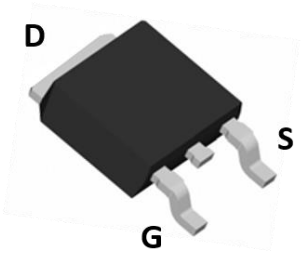
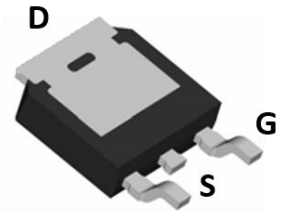
Leiditech

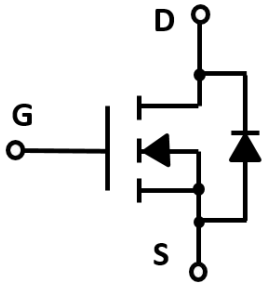
LMD20N06A

N-ChannelEnhancement Mode Field Effect Transistor





TO-252



Product Summary

- V_{DS} 60V
- I_D 20A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜43mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜47 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions
- Backlighting

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	20	A
	T_C=100℃		14	
Pulsed Drain Current [A]		I_{DM}	60	A
Total Power Dissipation	T_C=25℃	P_D	34	W
	T_C=100℃		17	W
Single Pulse Avalanche Energy [B]		E_{AS}	20	mJ
Thermal Resistance Junction-to-Case [C]		$R_{\theta JC}$	4.4	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+175	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
LMD20N06A	F2		2500	2500		13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA		60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	T_J=25℃			1	μA
			T_J=55℃			5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V				±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA		1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A			34	43	mΩ
		V_{GS}= 4.5V, I_D=10A			36	47	
Diode Forward Voltage	V_{SD}	I_S=10A,V_{GS}=0V			0.8	1.2	V
Maximum Body-Diode Continuous Current	I_S					20	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V,f=1MHZ			800		pF
Output Capacitance	C_{oss}				68		
Reverse Transfer Capacitance	C_{rss}				36		
Switching Parameters							
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=30V,I_D=10A			15		nC
Gate-Source Charge	Q_{gs}				2.4		
Gate-Drain Charge	Q_{gd}				2.5		
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=500A/us			23		
Reverse Recovery Time	t_{rr}				45		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=30V, I_D=2A,R_L=1Ω R_{GEN}=3Ω			5		
Turn-on Rise Time	t_r				39		
Turn-off Delay Time	$t_{D(off)}$				19		
Turn-off fall Time	t_f				7		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. T_j=25℃, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25Ω.

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

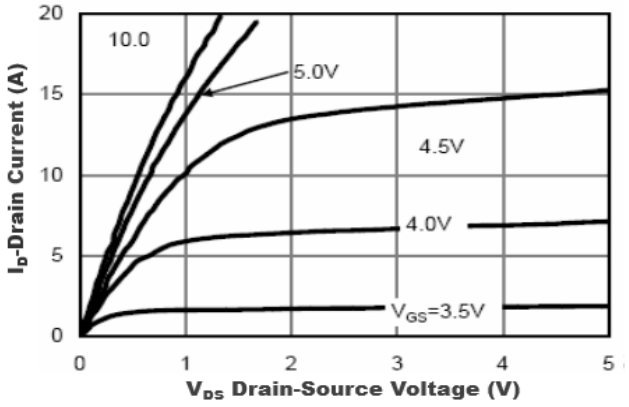


Figure1. Output Characteristics

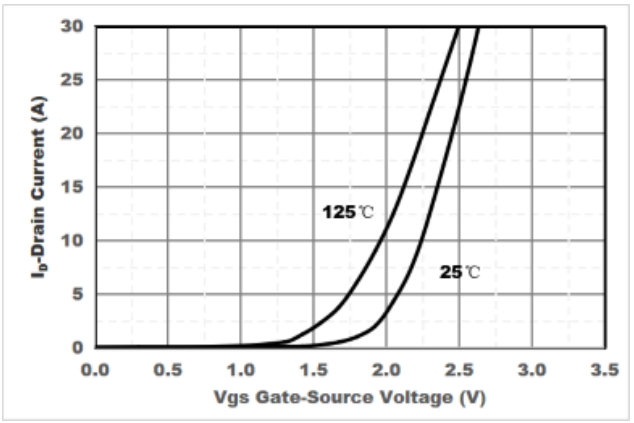


Figure2. Transfer Characteristics

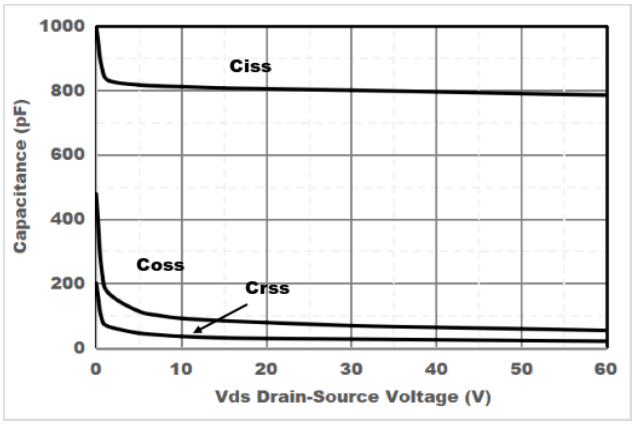


Figure3. Capacitance Characteristics

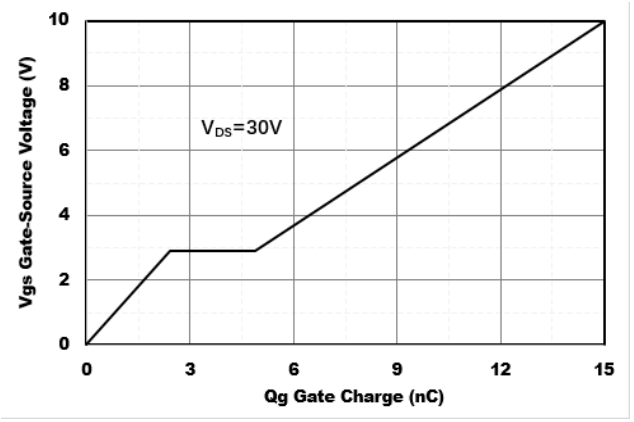


Figure4. Gate Charge

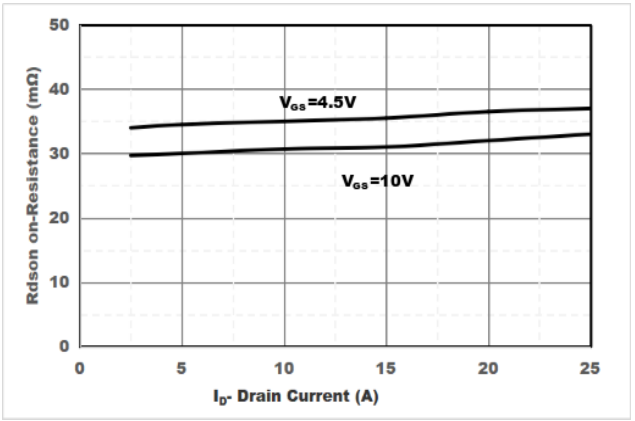


Figure5. Drain-Source on Resistance

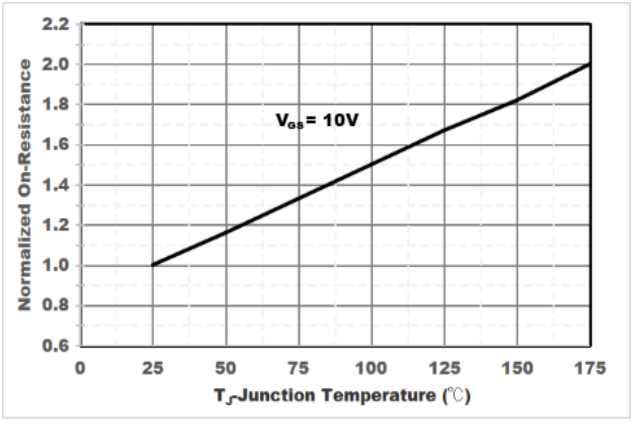


Figure6. Drain-Source on Resistance

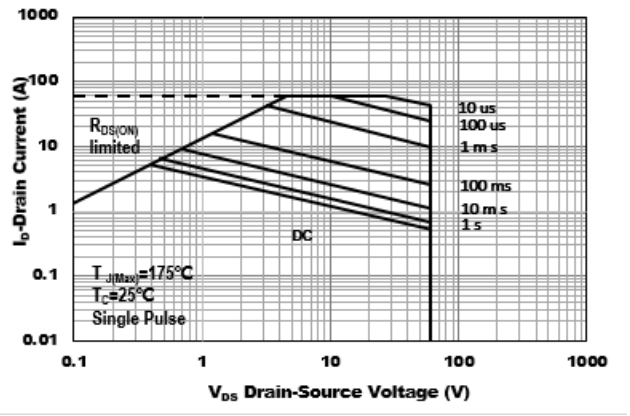


Figure7. Safe Operation Area

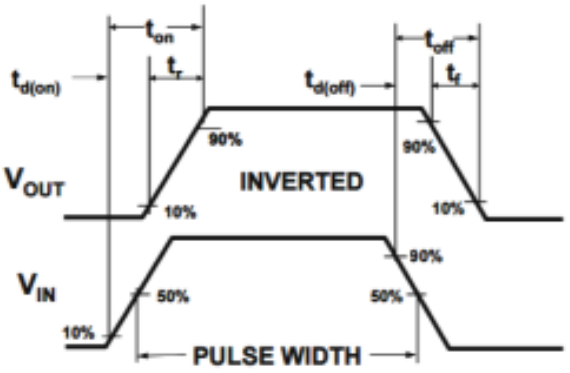
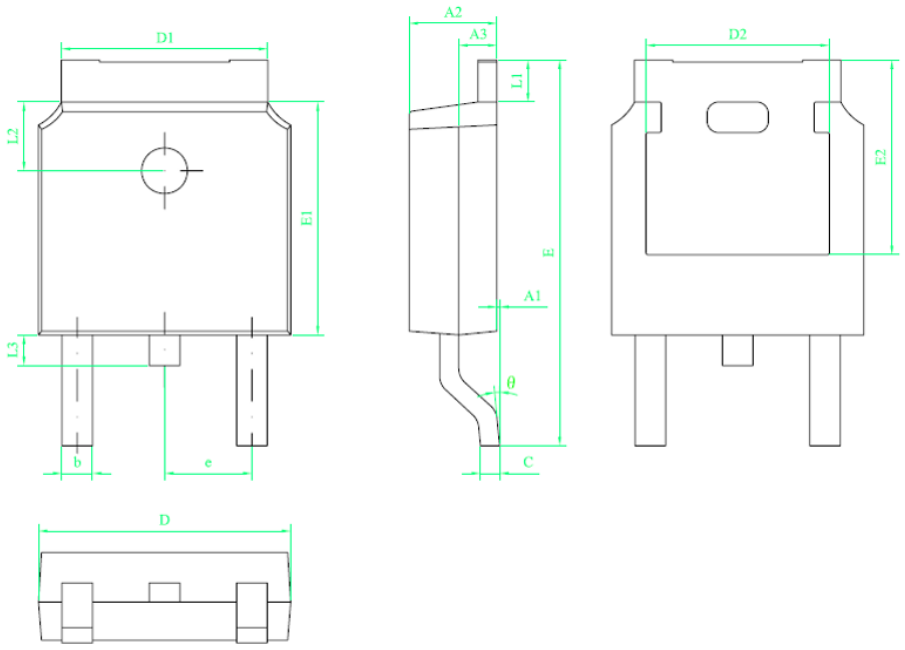


Figure8. Switching wave

■ TO-252 Package information



符 号	尺 寸		
	min	nom	max
A1	0	----	0.10
A2	2.20	2.30	2.40
A3	0.90	1.00	1.10
b	0.75	----	0.85
c	0.50	----	0.60
D	6.50	6.60	6.70
D1	5.30	5.40	5.50
D2	4.70	4.80	4.90
E	9.90	10.10	10.30
E1	6.00	6.10	6.20
E2	5.20	5.30	5.40
e	2.20	2.286	2.40
L1	0.90	----	1.25
L2	1.70	1.80	1.90
L3	0.60	0.80	1.00
θ	0°	----	8°

技术要求：
1. 树脂体不应有崩裂、缺损等缺陷；
2. 树脂上下部X、Y方向偏差不超过0.20；
3. 胶体两端留废胶总和宽度不超过0.50；
4. 所有单位为mm；

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