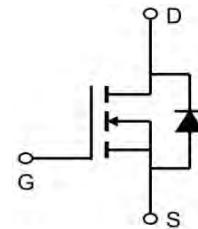


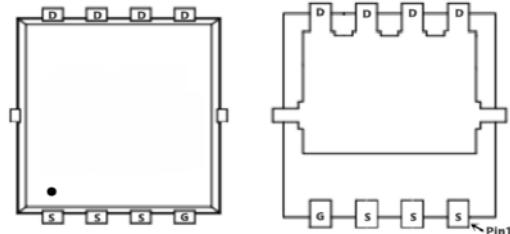
Description

These N-Channel enhancement mode power field effect transistors are using SGT technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.



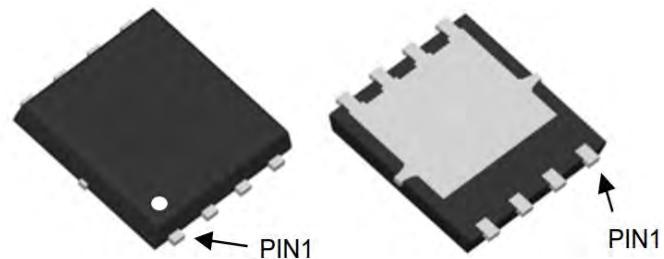
General Features

V_{DS}	40V
I_D (at $V_{GS}=10V$)	140A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	2.2mΩ(Max)



Application

- DC/DC Converter
- LED Backlighting
- Power Management Switches



Package Marking and Ordering Information

Device	Device Marking	Device Package	Reel Size	Tape width	Quantity
LM5D140N04	4996/5092SR	DFN5X6-8	-	-	5000 units

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted				
Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	V_{DS}	40	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Drain Current-Continuous	I_D (TC=25°C)	140	A	
	I_D (TC=100°C)	90	A	
Drain Current – Pulsed	I_{DM}	400	A	
Maximum Power Dissipation	P_D	73	W	
Single pulse avalanche energy	E_{AS}	529	mJ	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C	
Thermal Characteristics				
Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta JC}$		1.3	°C /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		62	°C /W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=40\text{V}, V_{\text{GS}}=0\text{V}$			1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0	1.7	3.0	V
$R_{\text{DS(ON)}}$	Drain-Source On-State Resistance	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=40\text{A}$		1.6	2.2	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=20\text{A}$		2.3	3.5	$\text{m}\Omega$
g_{fs}	Forward Transconductance	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=40\text{A}$		60		S
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$		4000		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			2.5		pF
SWITCHING PARAMETERS						
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}}=20\text{V}, I_{\text{D}}=40\text{A}, V_{\text{GS}}=10\text{V}, R_{\text{G}}=3\Omega$		15		nS
t_r	Turn-on Rise Time			25		nS
$t_{\text{d(off)}}$	Turn-Off Delay Time			68		nS
t_f	Turn-Off Fall Time			26		nS
Q_g	Total Gate Charge	$V_{\text{DS}}=20\text{V}, I_{\text{D}}=40\text{A}, V_{\text{GS}}=10\text{V}$		62		nC
Q_{gs}	Gate-Source Charge			12		nC
Q_{gd}	Gate-Drain Charge			10		nC
V_{SD}	Diode Forward Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{SD}}=1\text{A}$		0.72	1.3	V
R_g	Gate resistance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=0\text{V}, F=1\text{MHz}$		2		Ω
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Continuous Source Current	$V_{\text{G}}=V_{\text{D}}=0\text{V}$, Force Current			140	A
I_{SM}	Pulsed Source Current				280	A
t_{rr}	Reverse Recovery Time	$V_{\text{GS}}=0\text{V}, I_s=40\text{A}$,		48		nS
Q_{rr}	Reverse Recovery Charge	$\text{di/dt}=100\text{A}/\mu\text{s}$ $T_J=25^\circ\text{C}$		55		nC

Note:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. $V_{\text{DD}}=25\text{V}, V_{\text{GS}}=10\text{V}, L=0.5\text{mH}, I_{\text{AS}}=46\text{A}$, Starting $T_J=25^\circ\text{C}$
3. The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$.
4. Essentially independent of operating temperature.

Typical Electrical and Thermal Characteristics

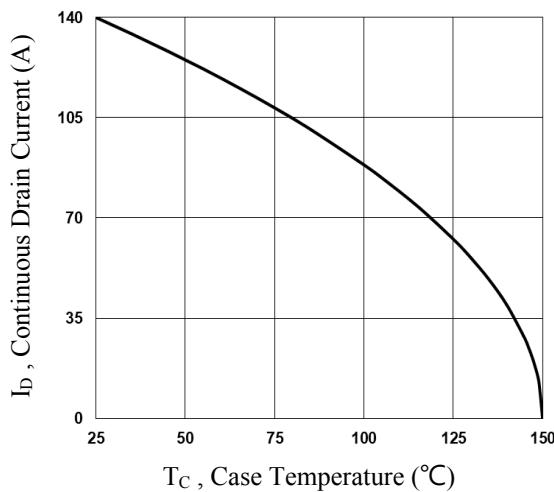


Fig.1 Continuous Drain Current vs. T_c

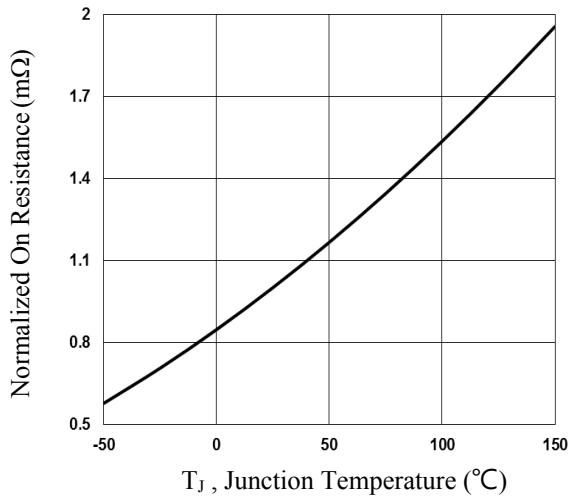


Fig.2 Normalized RDS(on) vs. T_j

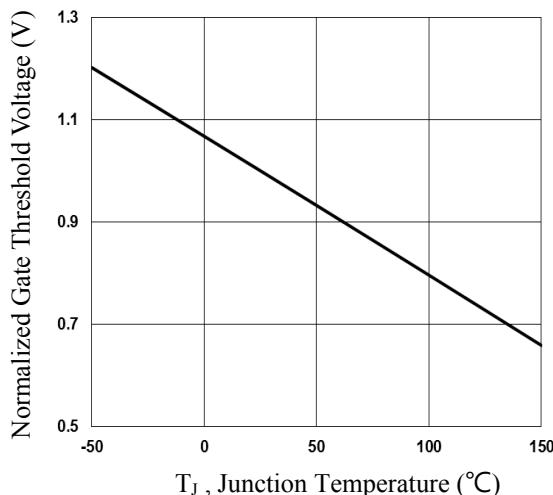


Fig.3 Normalized V_{th} vs. T_j

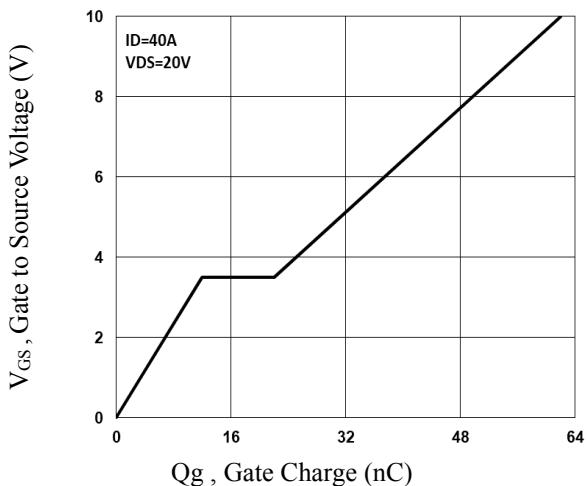


Fig.4 Gate Charge Characteristics

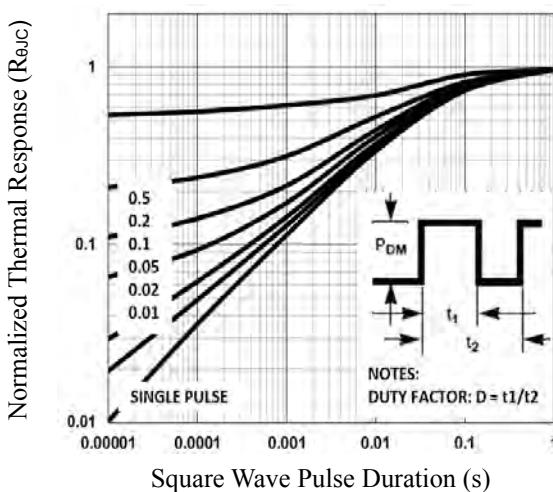


Fig.5 Normalized Transient Impedance

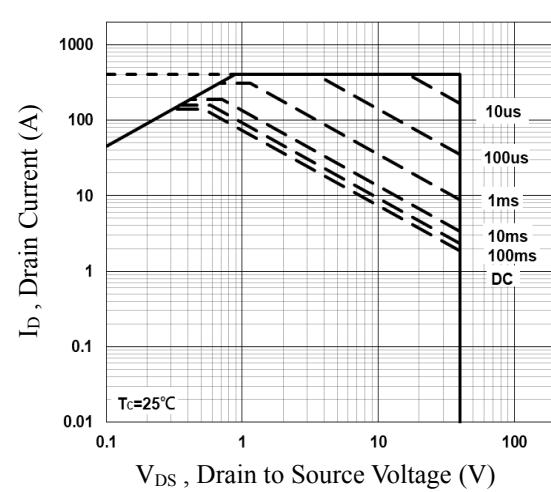


Fig.6 Maximum Safe Operation Area

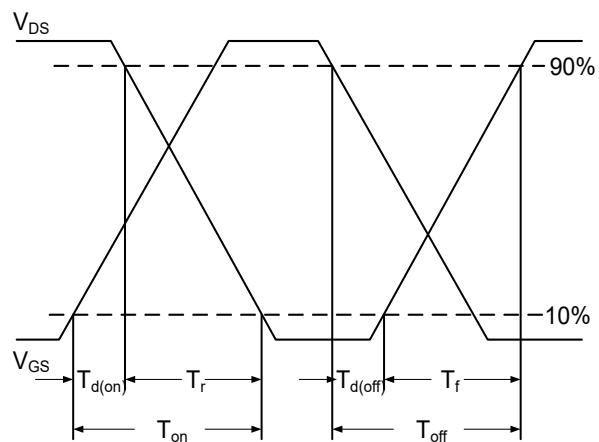


Fig.7 Switching Time Waveform

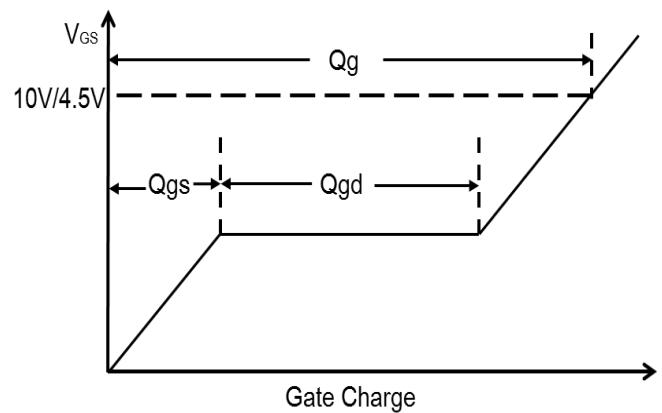
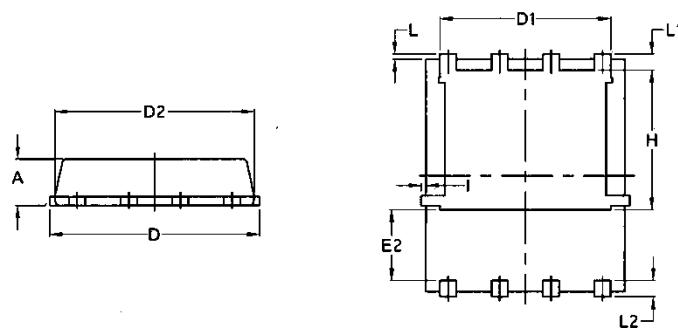
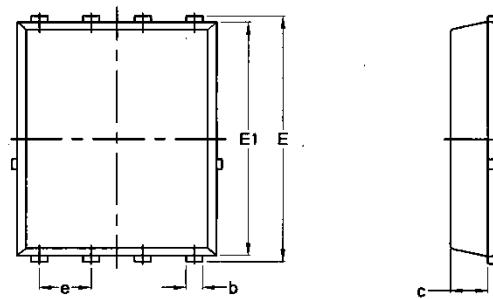


Fig.8 Gate Charge Waveform

Package Mechanical Data-DFN5*6-8-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

Shanghai Leiditech Electronic Co.,Ltd

Email: sale1@leiditech.com

Tel : +86- 021 50828806

Fax : +86- 021 50477059