Leiditech

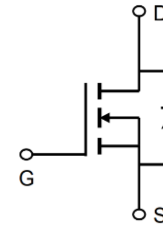
LMFB8N65

650V N-Channel Enhancement Mode MOSFET

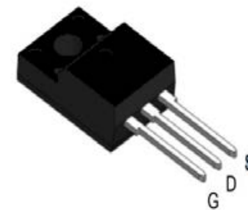
Description

The LMFB8N65 is CoolFET II MOSFET family that is utilizing charge balance technology for extremely low on-resistance and low gate charge performance. LMFB8N65 is suitable for applications which require superior power density and outstanding efficiency

Pin Configuration



Dimensions TO-220F



General Features

V_{DS} = 650V （Typ.730V） IDM =14A

$R_{DS(ON)}$ < 650mΩ @ V_{GS}=10V （Typ. 560mΩ）

Application

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)

Package Marking and Ordering Information

Device	Device Marking	Device Package	Reel Size	Tape width	Quantity
LMFB8N65	APJ14N65F	TO-220F	-	-	1000 units

Absolute Maximum Ratings (TC=25℃ unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	650	V
ID	Continuous Drain Current	8	A
IDM	Pulsed Drain Current (note1)	14	A
VGS	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	125	mJ
P_D	Power Dissipation (T_C = 25ºC)	25.5	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	4.9	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	49	ºC/W

Electrical Characteristics (TJ=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	650	700	--	V
ΔBV_{DSS} / ΔTJ	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C	--	0.7	--	V/°C
IDSS	Drain to source leakage current	V_{DS}=650V, V_{GS}=0V	--	--	1	uA
		V_{DS}=520V, T_C=125°C	--	--	50	uA
IGSS	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
VGS(TH)	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2.5	3.3	4.5	V
RDS(ON)	Drain to source on state resistance	V_{GS}=10V, I_D =3.2A	--	560	650	mΩ
Ciss	Input capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz	--	438	--	pF
Coss	Output capacitance		--	19.5	--	
Crss	Reverse transfer capacitance		--	1.32	--	
td(on)	Turn on delay time	V_{DS}=400V, I_D=3.2A，R_G=4.7Ω , V_{GS}=10V	--	84.8	--	ns
tr	Rising time		--	25.2	--	
td(off)	Turn off delay time		--	227.6	--	
t_f	Fall time		--	26.8	--	
Q_g	Total gate charge	V_{DS}=480V, V_{GS}=10V, I_D=3.2A	--	11		nC
Q_{gs}	Gate-source charge		--	2.1	--	
Q_{gd}	Gate-drain charge		--	5.6	--	
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	11	A
ISM	Pulsed source current		--	--	44	A
VSD	Diode forward voltage drop.	I_S=3.2A, V_{GS}=0V	--	0.7	1.5	V
T_{rr}	Reverse recovery time	I_S=3.2A, V_{GS}=0V, Vdd=400V, dI_F/dt=100A/us,	--	313	--	ns
Qrr	Reverse recovery Charge		--	0.877	--	uC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2、The EAS data shows Max. rating . L=0.5mH, IAS =3.2A, VDD =50V, RG=25Ω
3、The test condition is Pulse Test: ISD ≤ ID, di/dt = 100A/us, VDD≤ BVDSS, Starting at TJ =25℃
4、The power dissipation is limited by 150℃ junction temperature
5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Electrical and Thermal Characteristics

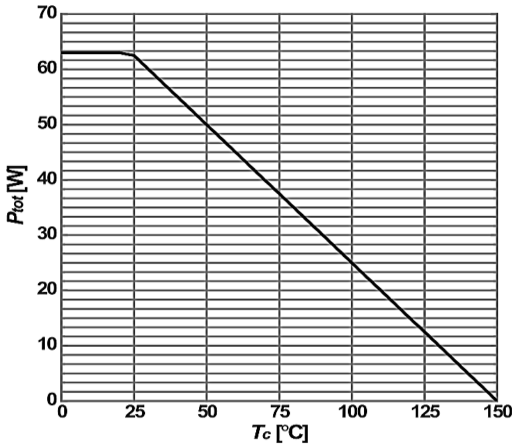


Figure1: Power dissipation (Non FullPAK)

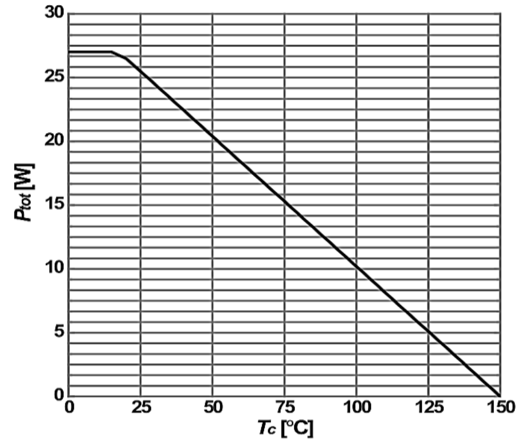


Figure2: Power dissipation (FullPAK)

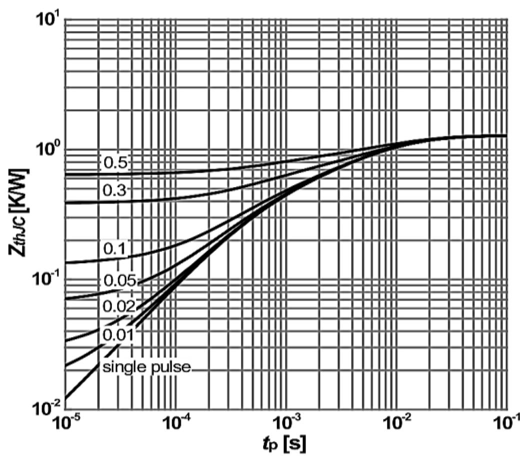


Figure3:Max. transient thermal impedance

Z_{thJC}=f(t_p); parameter: D= t_p/T

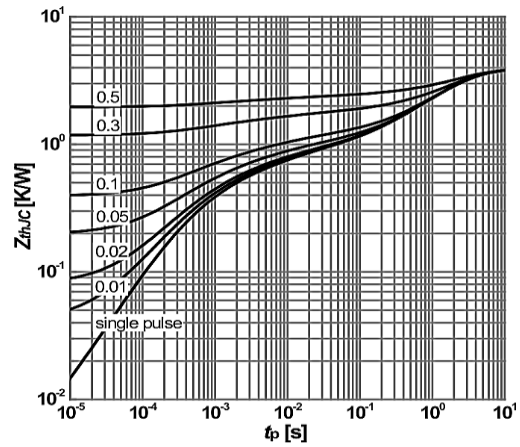


Figure4:Max. transient thermal impedance

Z_{thJC}=f(t_p); parameter: D= t_p/T

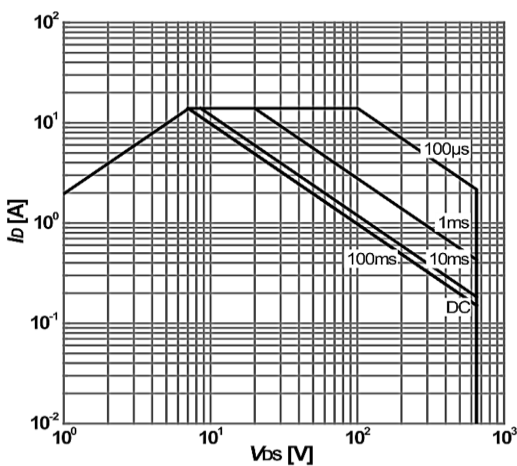


Figure5: Safe operating area (Non FullPAK)

I_D=f(V_{DS}); T_j=25°C; D=0; parameter: t_p

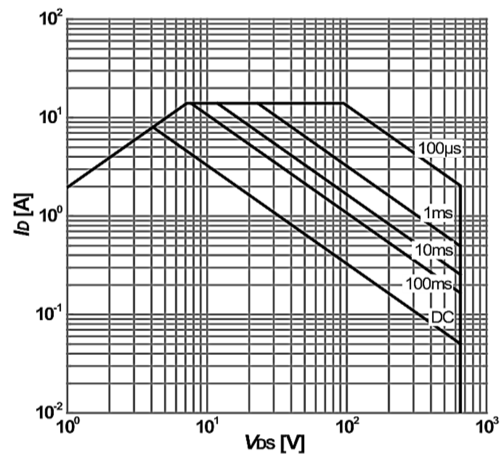


Figure6: Safe operating area (FullPAK)

I_D=f(V_{DS}); T_j=25°C; D=0; parameter: t_p

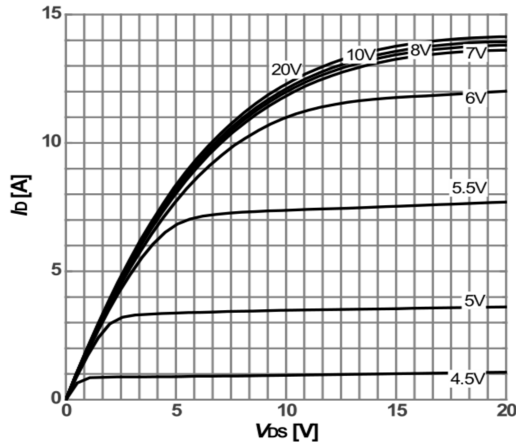


Figure 7: Typ. outp ut characteristics

I_D=f(V_{DS}); T_j=25°C; parameter: V_{GS}

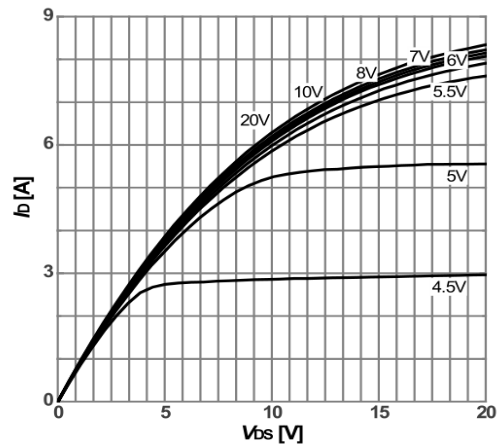


Figure8 : Typ. output characteristics

I_D=f(V_{DS}); T_j=125°C; parameter: V_{GS}

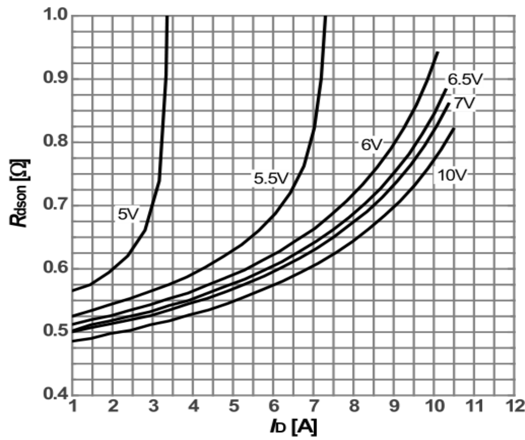


Figure9 : Typ. drain-source on-state resistance

R_{DS}(on)=f(I_D); T_j=25°C; parameter: V_{GS}

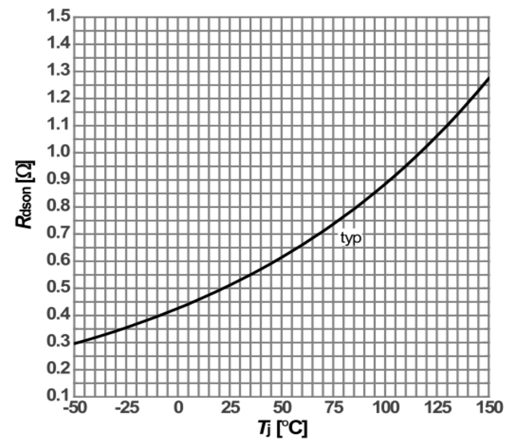


Figure 10: drain -source on-state resistance

R_{DS}(on)=f(T_j); I_D=3.2A; V_{GS}=10V

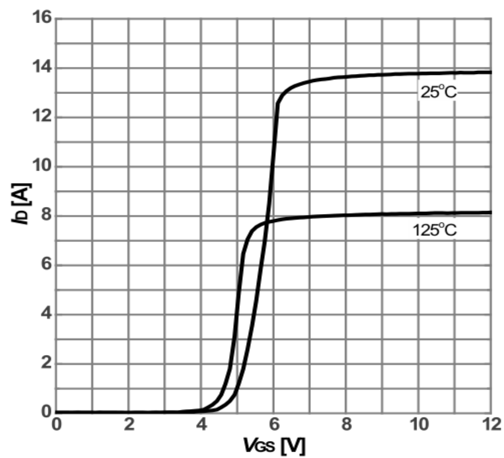


Figure 11: Type. transfer characteristics

I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

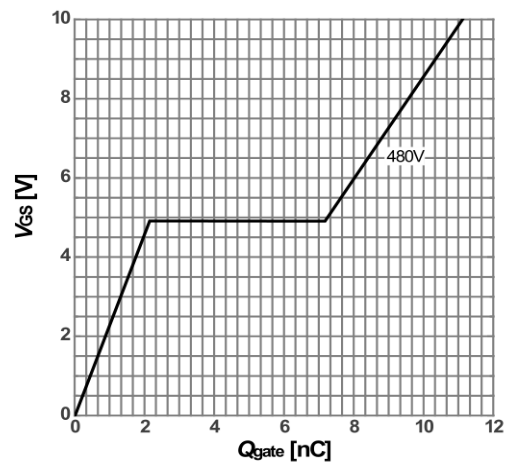
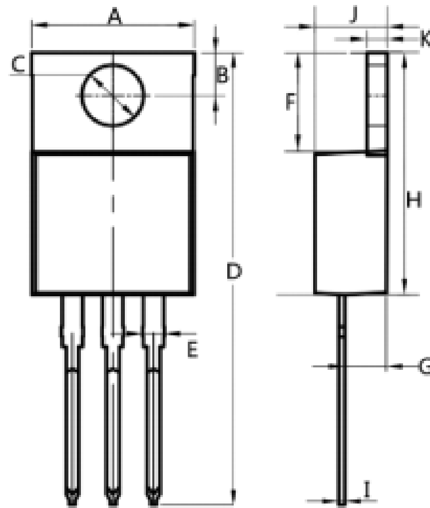


Figure 12: Type. gate charge

V_{GS}=f(Q_{gate}); I_D=3.2A pulsed; V_{DS}=480V

TO-220F Package Information



Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4
All Dimensions in millimeter		

NOTICE

Leiditech reserves the right to make modifications,enhancements,improvements,corrections or other changes without further notice to any product herein. Leiditech does not assume any liability arising out of the application or use of any product described herein.

Shanghai Leiditech Electronic Co.,Ltd
Email: sale1@leiditech.com
Tel : +86- 021 50828806
Fax : +86- 021 50477059