LMTVS2200DRVR

Flat-Clamp Surge Suppression Device 1-Line, 22V Surge Switch EOS Protection

Description

The flat-clamp surge suppressor LMTVS2200DRVR is used for EOS events in 22V and 24V systems. LMTVS2200DRVR has accurate and constant trigger voltage, excellent clamping performance and stable temperature characteristics, which can provide more comprehensive protection for the system. When the EOS event occurs, the trigger circuit accurately turns on the built-in field-effect transistor to release the current. The clamping voltage of the LMTVS2200DRVR is nearly constant over the specified peak pulse current range due to the very low on-resistance of the built-in leakage field effect transistor. Compared with the traditional TVS diode, LMTVS2200DRVR dissipates less surge energy, which can efficiently transfer overvoltage and overcurrent events to the ground through its own characteristics, thus avoiding increasing its own heat loss.

The LMTVS2200DRVR is designed to protect the power bus with operating voltages up to 22V and 24V, and its transient peak current reaches 70A (t_p = 8/20μs). The LMTVS2200DRVR uses a small DFN 2mm x 2mm x 0.68mm 6-lead package, which can significantly reduce the space of the circuit board compared with the traditional solution.

Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±30kV Contact Discharge
  - ±30kV Air Discharge
- High peak pulse current capability: 70A (tp = 8/20μs) per IEC 61000-4-5
- High EFT Withstand Voltage: ±4kV (100kHz and 5kHz, 5/50ns) IEC 61000-4-4
- High peak pulse current capability: 5A IEC 61643-321 (10/1000 μs)
- The clamping voltage is nearly constant across the rated peak pulse current range
- Operating voltage: 22V, 24V
- Low leakage: 1nA Typ @ 22V
- Low capacitance: 175pF Typ @ 22V

Application

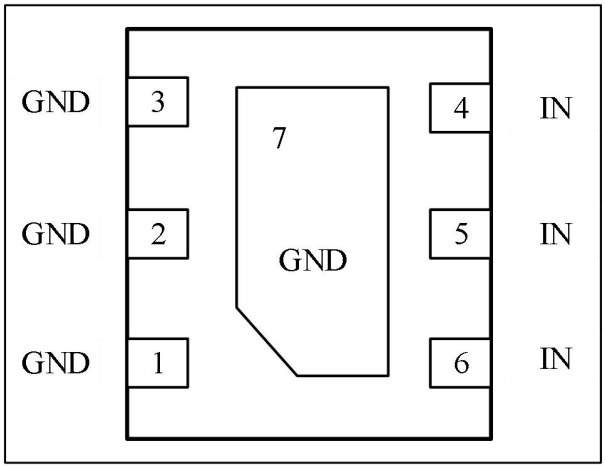
- USB PD
- USB Type-C
- Storage devices, industrial equipment
- Notebooks and Tablets
- Input protection of load switch and overvoltage protection chip

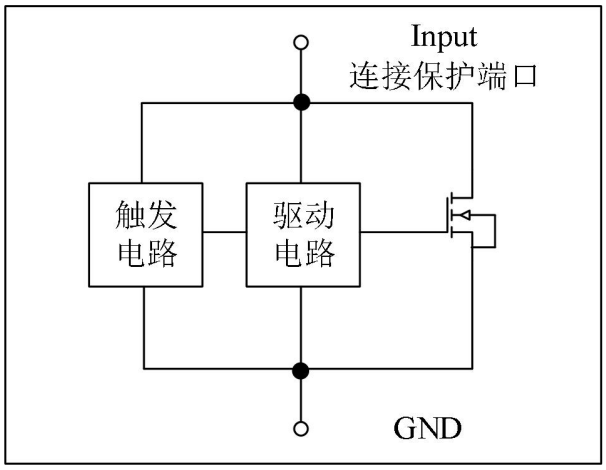
Ordering Information

Part Number	Package	Material	Packing	Quantity per reel	Flammability Rating	Reel Size
LMTVS2200DRVR	DFN 2mm X 2mm X 0.68 mm 6 lead	Halogen free	Tape & Reel	10,000 PCS	UL 94V-0	7 inches

Table-1 Ordering information

Pin Configuration





Absolute maximum rating (T = 25 ˚C)

Parameters	Symbol	Min.	Max.	Unit
IEC 61000-4-5 Current (8/20 μs) @25℃	P_{pk}	-	2100	W
IEC 61000-4-5 Power (8/20 μs)@25℃	I_{PP}		70	A
IEC 61643-321 Power (10/1000 μs) @25℃	P_{pk1}		150	W
IEC 61643-321 Current (10/1000 μs) @25℃	I_{PP1}		5	A
ESD (IEC61000-4-2 air discharge) @25℃	V_{ESD}	-	±30	kV
ESD (IEC61000-4-2 contact discharge) @25℃	V_{ESD}	-	±30	kV
Operating temperature	T_{OP}	-40	125	℃
Storage temperature	T_{STG}	-55	150	℃

Table-2 Absolute maximum rating

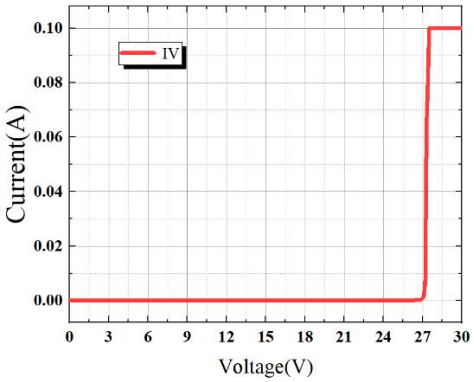
Electrical characteristics At TA = 25°C unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse operating voltage	V_{RWM}				24	V
Reverse breakdown voltage	V_{BR}	I_T=1mA；T=25°C	25	27	27.5	V
Reverse leakage	I_R	V_{RWM}=22V；T=25°C		1	100	nA
Forward voltage	V_F	I_T=1mA；T=25°C		0.52	0.7	V
Clamping voltage	V_{CL}	I_{PP}=1A; t_p=8/20us；T=25°C		27	27.5	
	V_{CL}	I_{PP}=20A; t_p=8/20us；T=25°C		27.4	27.9	V
	V_{CL}	I_{PP}=40A; t_p=8/20us；T=25°C		27.8	28.3	V
	V_{CL}	I_{PP}=70A; t_p=8/20us；T=25°C		29.4	29.9	V
On resistance	R_{DYN}*	t_p=8/20us；T=25°C			40	mΩ
Junction capacitance	C_J	V_R=22V; f=1MHz；T=25°C		175		pF

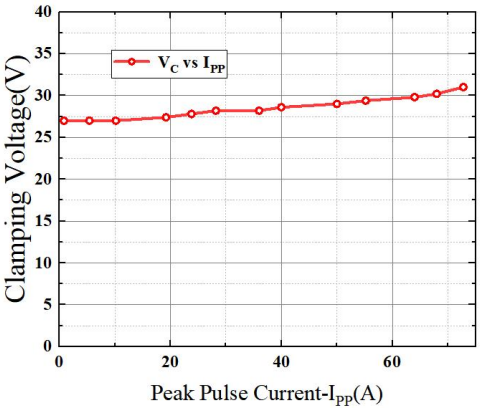
Table-2 Electrical characteristics

* On-resistance test is 1A-70A (t_p = 8/20 μs).

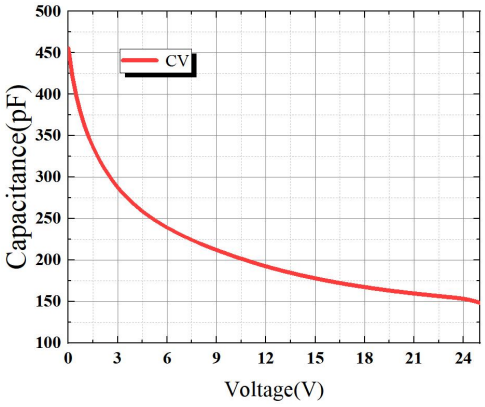
Typical characteristics



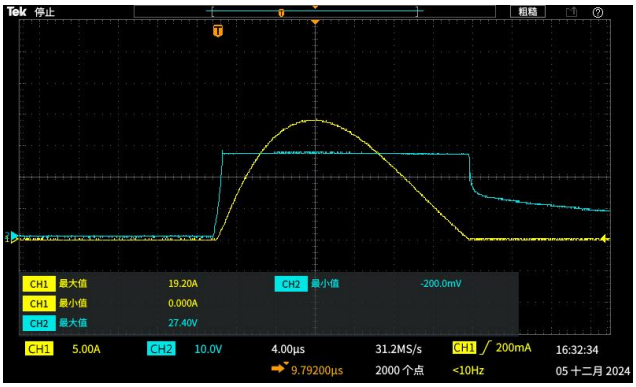
IV characteristics



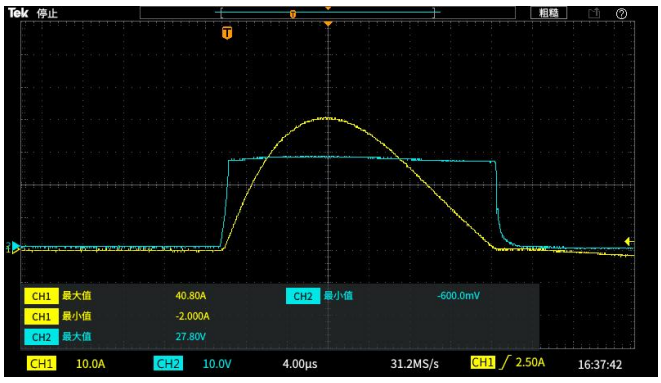
V_C vs. I_{PP}



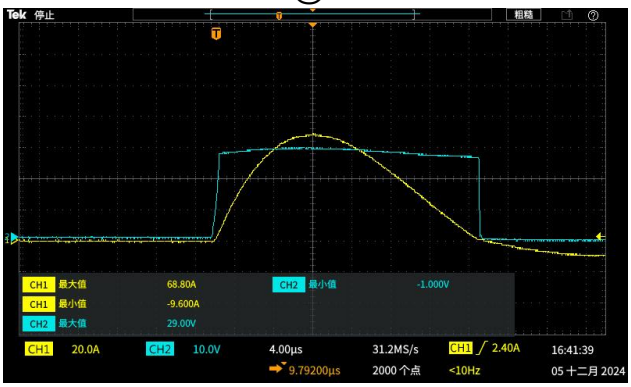
电容 vs.偏置电压



27.4V@19.20A



27.8V@40.8A



29V@68.8A

Application information

General description

Flat clamp surge suppressors (TDS) are designed to provide high energy EOS protection. Compared with traditional TVS diodes, it has excellent clamping performance and temperature characteristics.

The traditional TVS diode based on pn junction has a fixed dynamic resistance RDYN. The clamping voltage of TVS is $V_C = V_{BR} + I_{PP} * R_{DYN}$. The dynamic resistance is a fixed value, so the clamping voltage increases with the increase of I_{PP}, which causes the clamping voltage to rise linearly in the peak pulse current range. In addition, the ability of conventional TVS diodes to absorb transient currents is related to the junction area and the junction (ambient) temperature. When TVS absorbs or dissipates surge energy, its own temperature will increase, the clamping voltage will increase significantly, and the transient peak current IPP will decrease.

The flat clamp surge suppressor uses the surge rated FET as the main protection element (Figure 1), which is composed of a precision trigger circuit, a drive circuit, and a rated surge FET (Figure 2). When the trigger circuit detects an EOS event, the trigger circuit activates the driver circuit and turns on the field effect transistor, which effectively transfers the transient current to ground.

As the I_{PP} increases, the R_{DYN} of the FET is reduced to a negligible value, which makes the clamping voltage approximately the same as the breakdown voltage of the trigger circuit. Therefore, the clamping voltage of LMTVS2200DRVR is almost constan t in the range of rated peak pulse current. In addition , the clamping voltage within the normal operating temperature range is also stable.

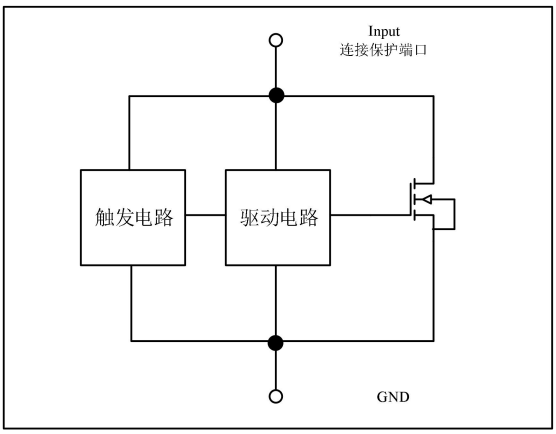


Figure 1 TDS Block Diagram

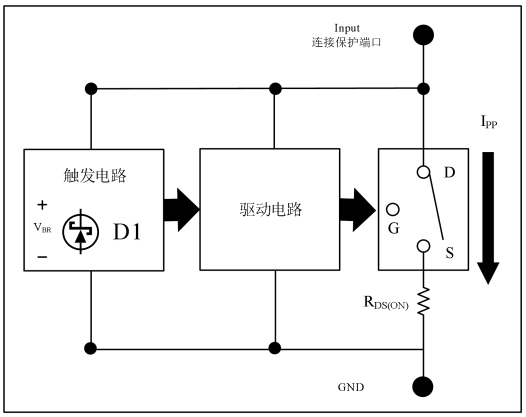


Figure 2 Working principle of TDS

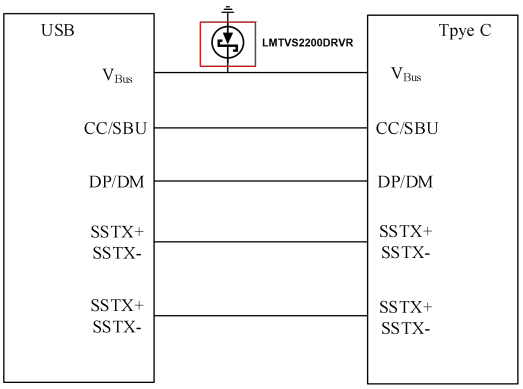


Figure 3 USB Type-C Application Solution

The typical application of LMTVS2200DRVR is to protect the USB Type-C interface, and the working voltage of the USB Type-C bus with PD (power delivery) function is up to 22V or 24V. If the voltage on the bus is greater than its designed parameters, the controller of the USB PD may be damaged.

TVS diodes are often used to protect the bus, but designers are often forced to choose devices with larger peak pulse currents to keep the clamp voltage below the breakdown threshold of the PD controller. In addition, the clamping voltage of the TVS device increases with the increase of temperature, so it is difficult for designers to estimate the protection capability at higher operating temperatures. The LMTVS2200DRVR is a more reliable solution because it maintains a lower clamping voltage over the rated peak pulse current and operating temperature range.

The LMTVS2200DRVR can also be used to protect load switches, overvoltage protection chips, and electronic fuse inputs in applications such as industrial equipment, remote instrumentation, robotics, USB PD, and iot devices (Figure 4). In this case, LMTVS2200DRVR not only protects downstream components from lightning, ESD and EOS events, it also protects the load switch by keeping the clamp voltage below the breakdown threshold of the FET inside the switch.

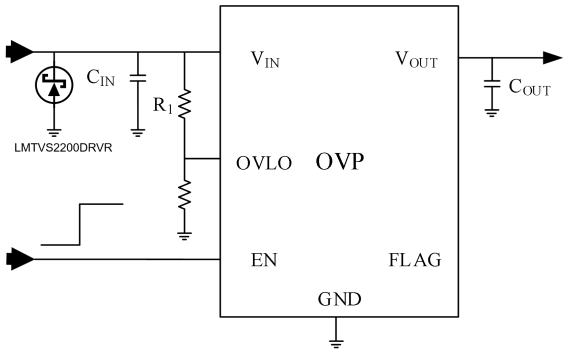
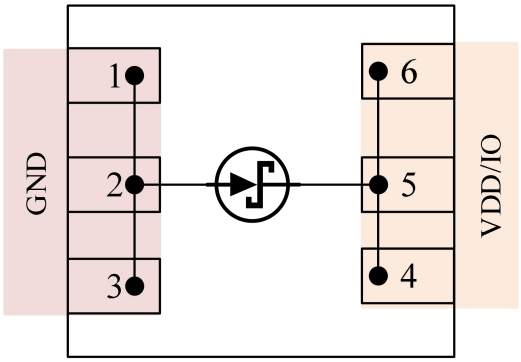


Figure 4. Input protection of load switch and overvoltage protection chip

Pin configuration

LMTVS2200DRVR is 2mm x 2mm x 0.68mm, 6-pin QFN package.

The protected bus is connected to pins 4,5, and 6. Pins 1,2 and 3 are connected to GND. All pins must be connected to obtain the maximum peak pulse current processing capability.



1,2,3	GND
4,5,6	VDD/IO

Figure 5. Pin Configuration and Description

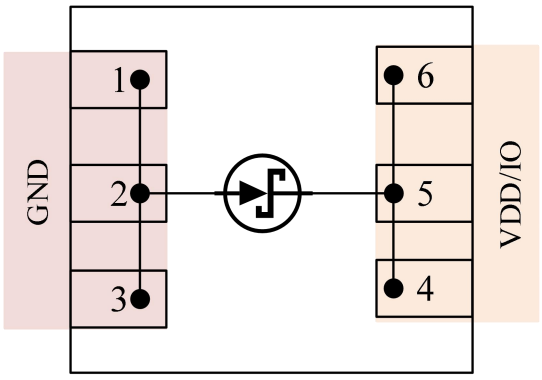


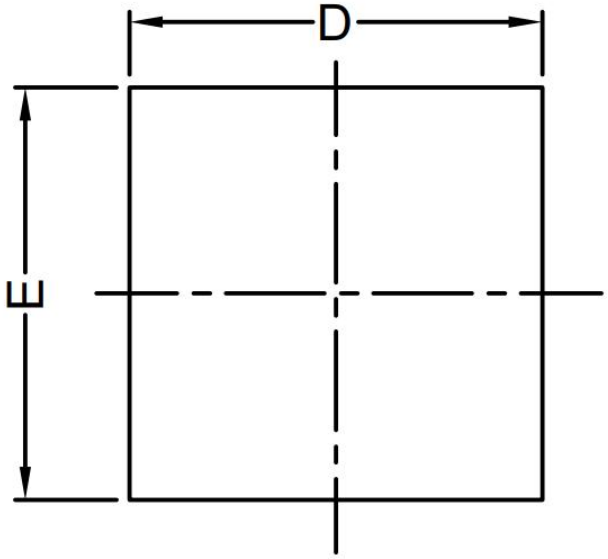
Figure 6. Recommended PCB Layout

Layout recommendations

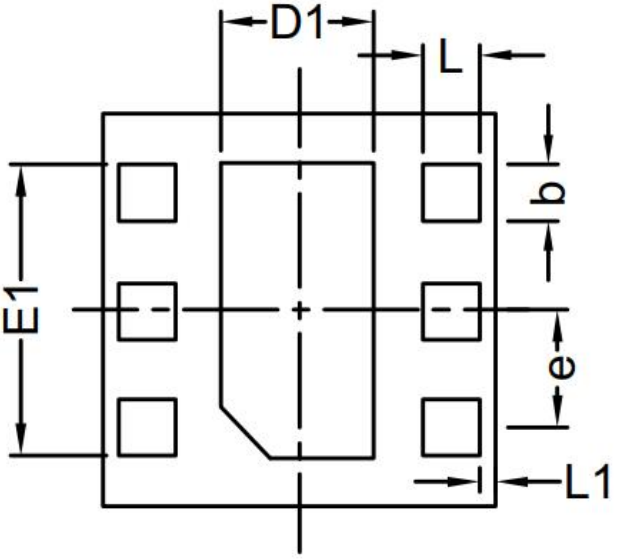
Figure 6 shows the recommended layout of LMTVS2200DRVR. All I / O pins (pins 4, 5 and 6) are connected by a straight line. All I / O pins must be connected to achieve maximum surge performance.All GND pins (pins 1, 2, and 3) must also be connected to obtain maximum surge currentcapability. If the ground is on different PCB layers, it is recommended to use multiple holes for connection, which helps to reduce the parasitic inductance to theground.

Encapsulate information

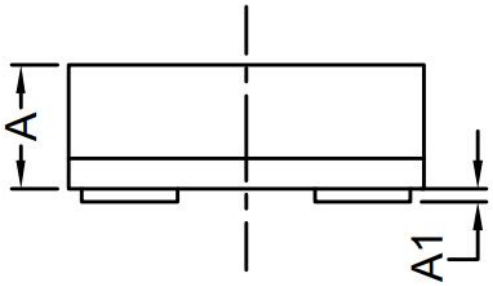
POD(A)



TOP VIEW



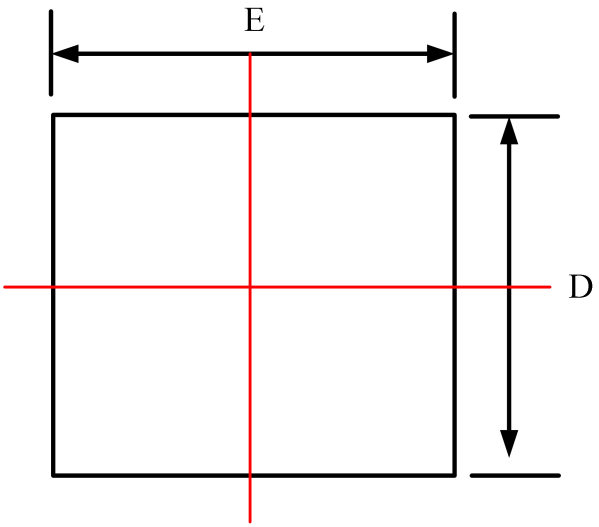
BOTTOM VIEW



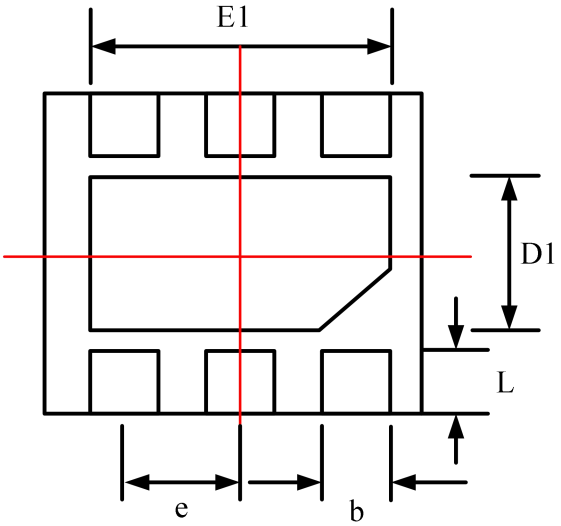
SIDE VIEW

COMMON DIMENSION (MM)			
PKG DFN2.0*2.0-6L			
REF.	MIN.	NOM.	MAX
A	0.63	0.68	0.73
A1	0.02	0.03	0.04
D	1.95	2.00	2.05
E	1.95	2.00	2.05
L	0.20	0.25	0.3
L1	0.00	0.05	0.08
b	0.25	0.30	0.35
e	0.65		
D1	0.95	1.00	1.05
E1	1.55	1.60	1.65

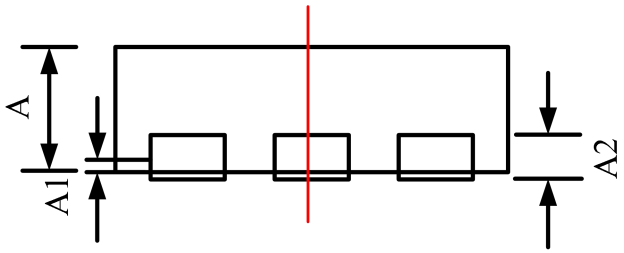
POD(B)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSION (MM)			
PKG DFN2.0*2.0-6L			
REF.	MIN.	NOM.	MAX
A	0.50	0.55	0.6
A1	0.00	0.03	0.05
A2		0.15REF	
D	1.95	2.00	2.05
E	1.95	2.00	2.05
E1	1.55	1.60	1.65
L	0.20	0.25	0.30
b	0.25	0.30	0.35
e		0.65bsc	
D1	0.95	1.00	1.05

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