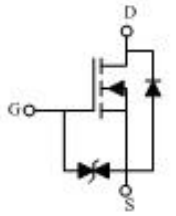
LM3134KM3

20V N-Channel Enhancement Mode MOSFET

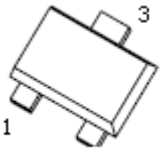
Features

- V_{DS} = 20V I_D =0.75A
- $R_{DS(ON)}$ <400mΩ@ V_{GS}=4.5V
- Lead Free Product is Acquired
- Surface Mount Package
- N-Channel Switch with Low $R_{DS(ON)}$
- Operated at Low Logic Level Gate Drive
- Typical ESD Protection HBM Class 2KV

Inner Equivalent Principium Chart



Pin Assignment



1. GATE
2. SOURCE
3. DRAIN

Applications

- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

Package Marking and Ordering Information

Marking	Part Number	Package	Packing	Quantity
KF	LM3134KM3	SOT-723	Reel	8,000 units

Absolute Maximum Ratings (T_a=25℃unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Typical Gate-Source Voltage	V_{GS}	±10	V
Continuous Drain Current (note 1)	I_D	0.75	A
Pulsed Drain Current (t_p=10μs)	I_{DM}	1.8	A
Power Dissipation (note 1)	P_D	150	mW
Thermal Resistance from Junction to Ambient (note 1)	$R_{\theta JA}$	833	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~+150	℃
Lead Temperature for Soldering Purposes(1/8” from case for 10 s)	T_L	260	℃

Electrical Characteristics (T_a=25℃unless otherwise noted)

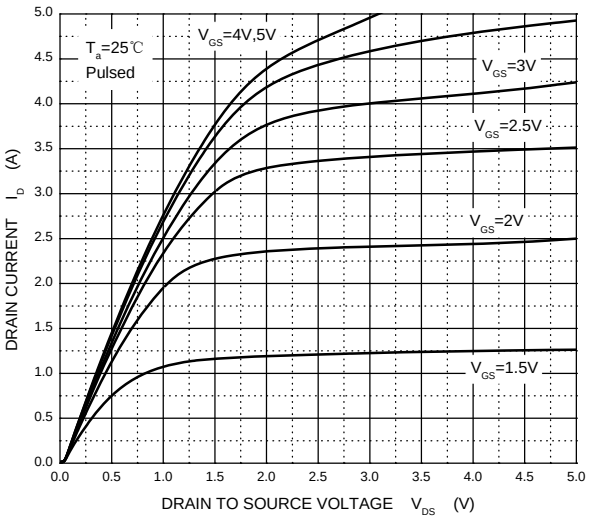
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHARACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =20V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±10V, V_{DS} = 0V			±20	μA
Gate threshold voltage (note 2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.35	0.7	1	V
Drain-source on-resistance (note 2)	$R_{DS(on)}$	V_{GS} =4.5V, I_D =0.5A		270	400	mΩ
		V_{GS} =2.5V, I_D =0.5A		320	500	mΩ
		V_{GS} =1.8V, I_D =0.45A		390	800	mΩ
Forward transconductance (note 2)	g_{FS}	V_{DS} =10V, I_D =0.8A		1.6		S
Diode forward voltage	V_{SD}	I_S=0.15A, V_{GS} = 0V			1.2	V
DYNAMIC CHARACTERISTICS (note 4)						
Input capacitance	C_{iss}	V_{DS} =16V,V_{GS} =0V,f =1MHz		79	120	pF
Output capacitance	C_{oss}			13	20	pF
Reverse transfer capacitance	C_{rss}			9	15	pF
SWITCHING CHARACTERISTICS (note 4)						
Turn-on delay time (note 3)	$t_{d(on)}$	V_{GS}=4.5V,V_{DS}=10V, I_D =500mA,R_{GEN}=10Ω		6.7		ns
Turn-on rise time (note 3)	t_r			4.8		ns
Turn-off delay time (note3)	$t_{d(off)}$			17.3		ns
Turn-off fall time (note 3)	t_f			7.4		ns
Total Gate Charge (note 3)	Q_g	V_{DS} =10V,V_{GS} =4.5V,I_D =0.25A		750		pC
Gate-Source Charge (note 3)	Q_{gs}			75		pC
Gate-Drain Charge (note 3)	Q_{gd}			225		pC

Notes :

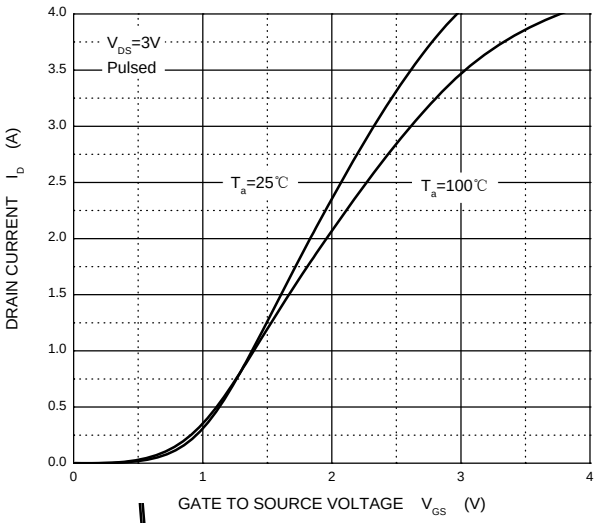
1. Surface mounted on FR4 board using the minimum recommended pad size.
2. Pulse Test : Pulse Width=300μs, Duty Cycle=2%.
3. Switching characteristics are independent of operating junction temperatures.
4. Guaranteed by design, not subject to producting.

Typical Performance Characteristics

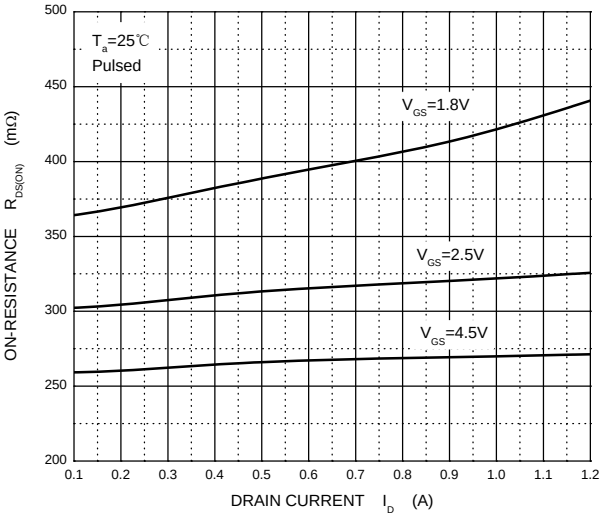
Output Characteristics



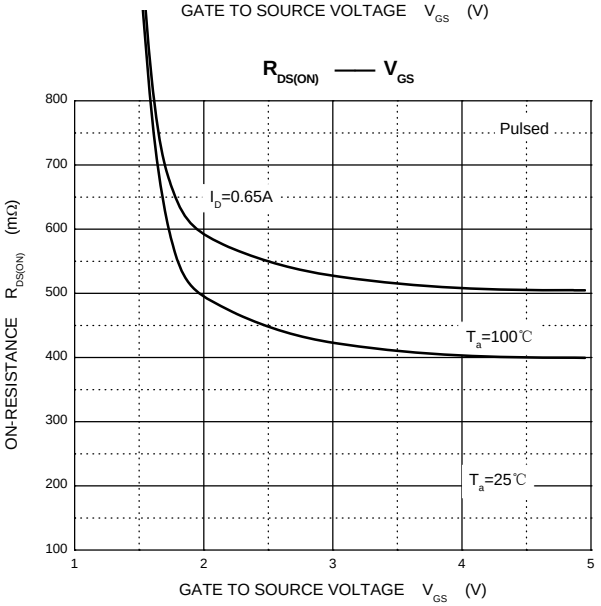
Transfer Characteristics



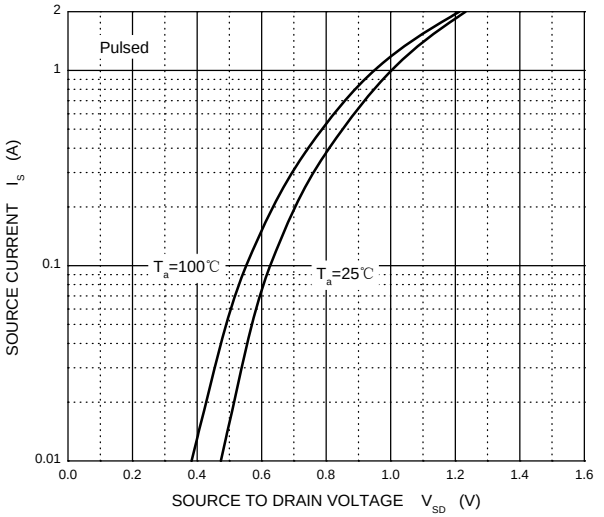
$R_{DS(ON)}$ —— I_D



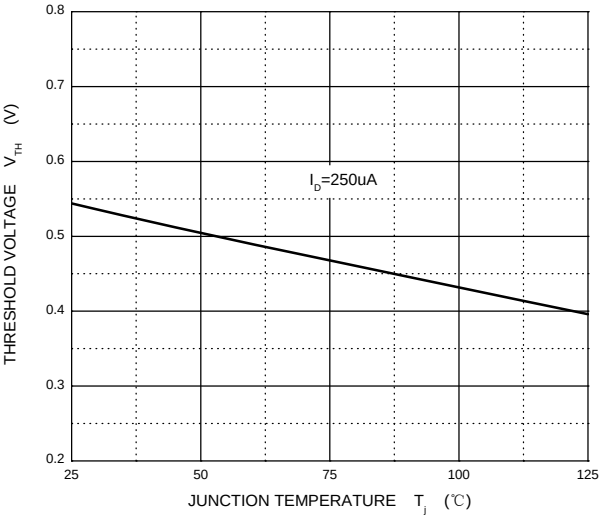
$R_{DS(ON)}$ —— V_{GS}



I_S —— V_{SD}



Threshold Voltage



Test Circuit & Waveform

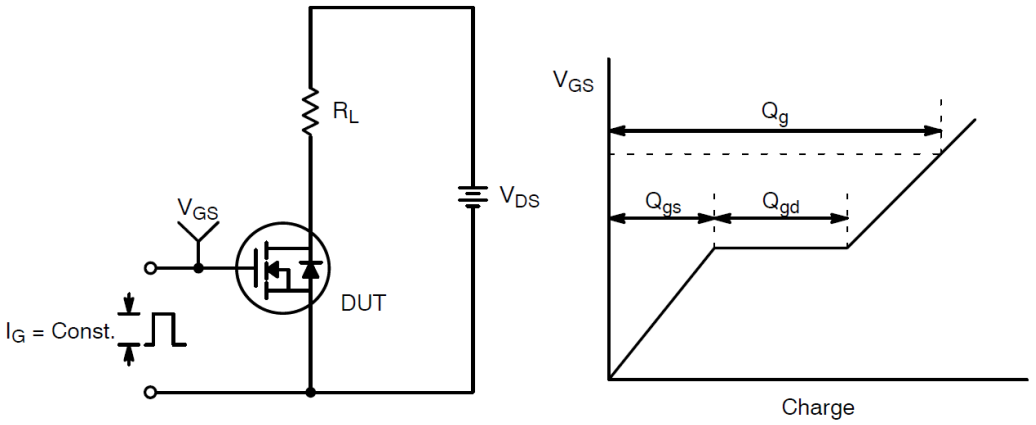


Figure 7 : Gate Charge Test Circuit & Waveform

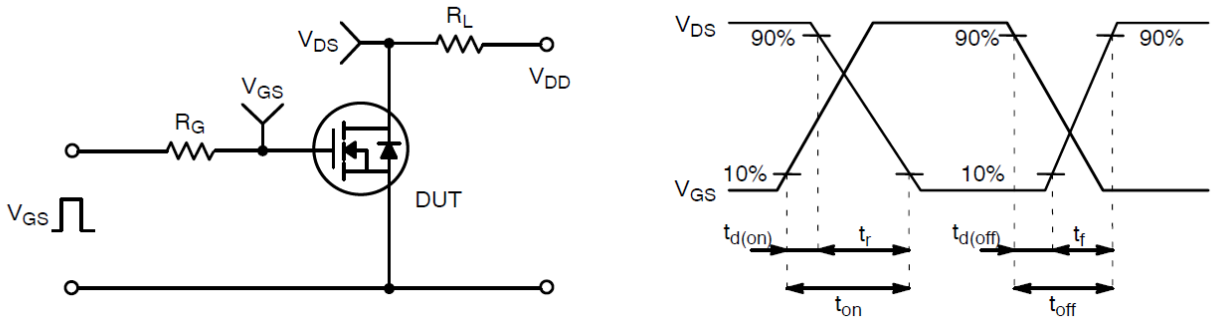


Figure 8 : Resistive Switching Test Circuit & Waveforms

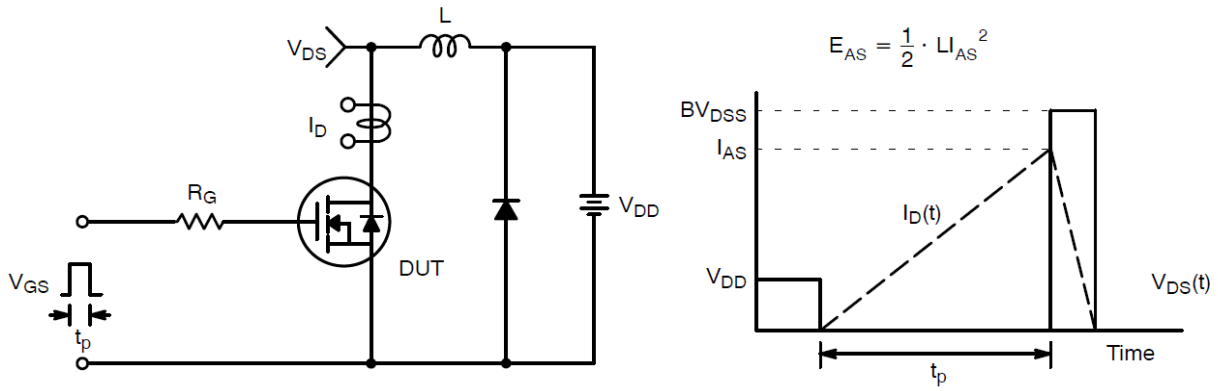
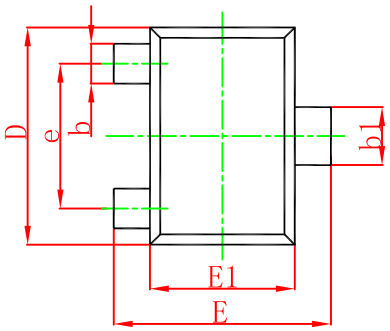
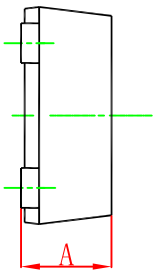
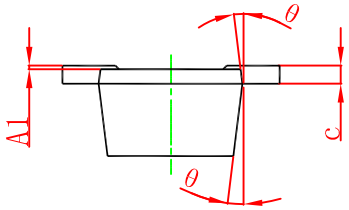


Figure 9 : Unclamped Inductive Switching Test Circuit & Waveforms

SOT-723 Package Outline Dimensions

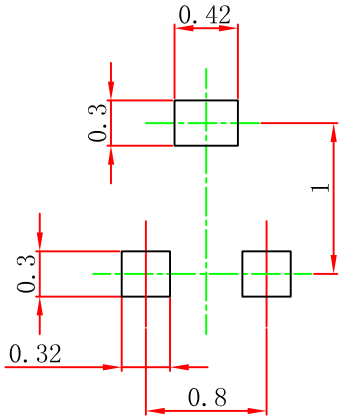






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.430	0.500	0.017	0.020
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
b1	0.270	0.370	0.011	0.015
c	0.080	0.150	0.003	0.006
D	1.150	1.250	0.045	0.049
E	1.150	1.250	0.045	0.049
E1	0.750	0.850	0.030	0.033
e	0.800TYP.		0.031TYP.	
θ	7° REF.		7° REF.	

SOT-723 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

Shanghai Leiditech Electronic Technology Co., Ltd.
Email: sale1@leiditech.com
Tel : +86- 021 50828806
Fax : +86- 021 50477059