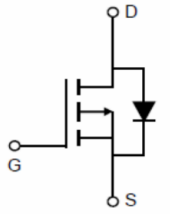
LMTL2P06A

-60V P-Channel Enhancement Mode MOSFET

General Description

The LMTL2P06A uses SGT technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOT-23, which accords with the ROHS standard and Halogen Free standard.

Inner Equivalent Principium Chart

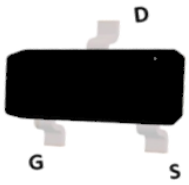


Features

V_{DS} = -60V I_D = -2A

$R_{DS(ON)}$ < 165mΩ @ V_{GS}=-10V

Pin Assignment



Applications

- DC-DC Converter
- Portable Equipment
- Power Management

Package Marking and Ordering Information

Marking	Part Number	Package	Packing	Qty.
S6T8A	LMTL2P06A	SOT-23	Reel	3000 Pcs

Absolute Maximum Ratings

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		-60	V
I_D	Continuous Drain Current	T_A=25℃	-2.0	A
	Continuous Drain Current	T_A=100℃	-1.3	A
I_{DM}[a1]	Pulsed Drain Current		-8.0	A
V_{GS}	Gate-to-Source Voltage		±20	V
P_D	Power Dissipation		1.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	℃
T_L	Maximum Temperature for Soldering		260	℃

Thermal Characteristics

Symbol	Parameter	Value	Units
$R_{\theta JA}$[a2]	Thermal Resistance, Junction-to-Ambient	83	℃/W

Electrical Characteristic (T_J = 25 °C, unless otherwise specified)

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-60	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=-60V, V_{GS}=0V	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=-20V, V_{DS}=0V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=+20V, V_{DS}=0V	--	--	-100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.1	-1.6	-2.0	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=-10V, I_D=-2.0A	--	135	165	mΩ
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=-4.5V, I_D=-1.5A	--	175	220	mΩ

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS} =0V V_{DS} =-30V f =1.0MHz	--	131	--	pF
C_{oss}	Output Capacitance		--	32	--	
C_{rss}	Reverse Transfer Capacitance		--	3.2	--	
R_G	Gate resistance	V_{GS}=0V,V_{DS} =0V,f=1MHz	--	36	--	Ω

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =-2.0A V_{DS} =-30V V_{GS} =-10V R_G =3.3Ω	--	18	--	ns
t_r	Rise Time		--	5.3	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	39	--	
t_f	Fall Time		--	3.4	--	
Q_g	Total Gate Charge	V_{GS} =-10V V_{DS} =-30V I_D =-2.0A	--	3.9	--	nC
Q_{gs}	Gate to Source Charge		--	0.5	--	
Q_{gd}	Gate to Drain Charge		--	0.6	--	

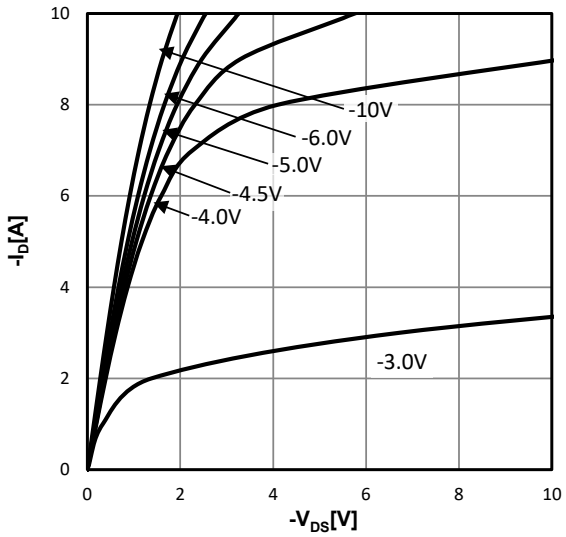
Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	T_A =25 °C	--	--	-2.0	A
V_{SD}	Diode Forward Voltage	I_S=-2.0A, V_{GS}=0V	--	--	-1.2	V

a1：Repetitive rating; pulse width limited by maximum junction temperature

a2：Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 μm thick) copper area for drain connection.

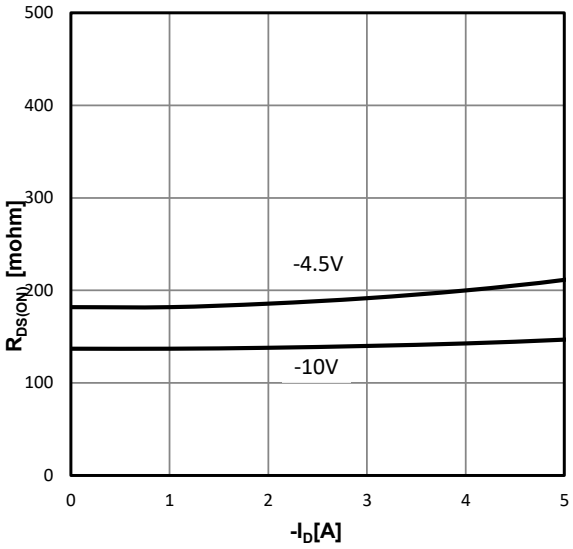
Characteristics Curve

Figure 1: Typ. output characteristics



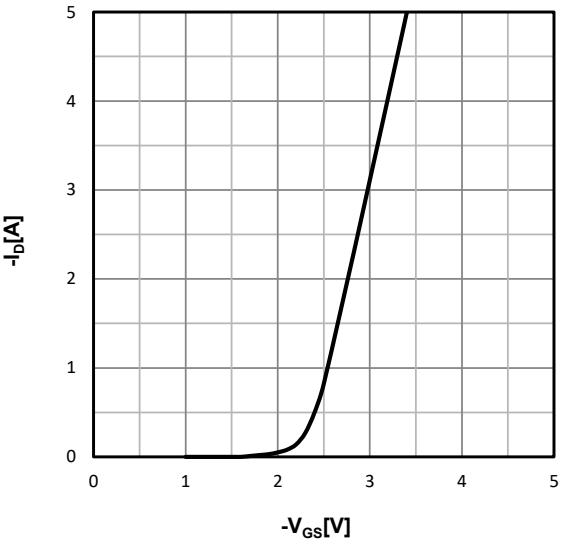
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}

Figure 2: Typ. drain-source on resistance



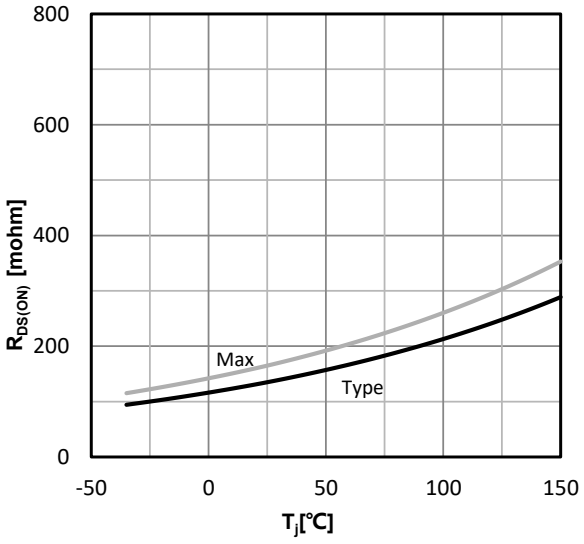
$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

Figure 3: Typ. transfer characteristics



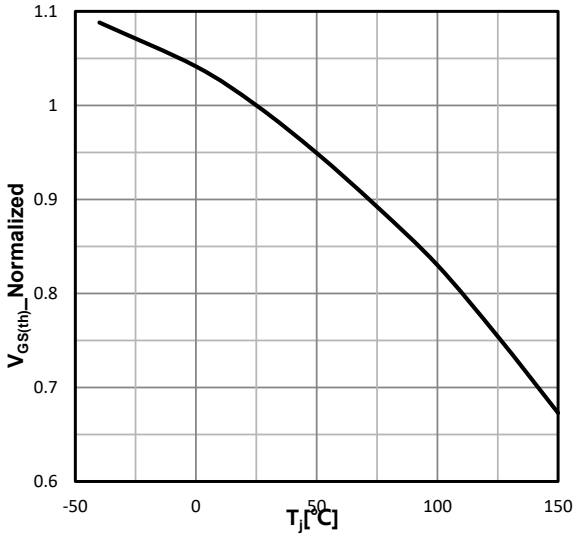
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS}(on)max$;

Figure 4: drain-source on resistance



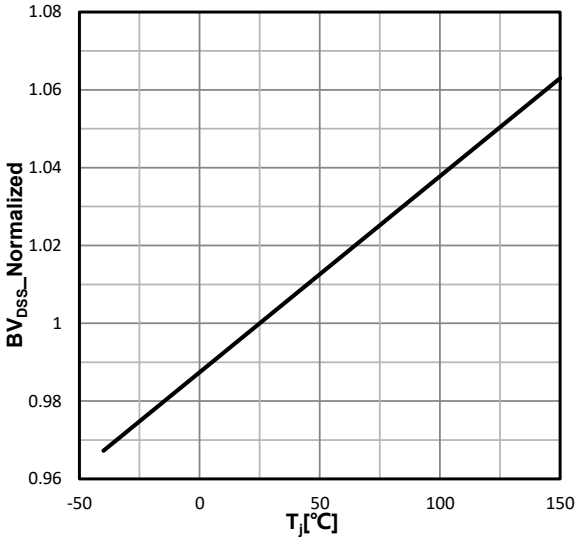
$R_{DS(on)}=f(T_j)$, I_D=-2.0A, V_{GS}=-10V;

Figure 5: Typ. gate threshold voltage



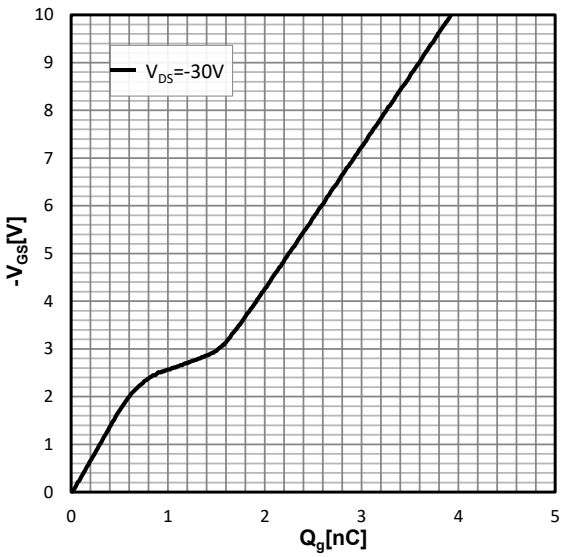
$V_{GS}=f(T_j)$,$V_{GS}=V_{DS}$,I_D=-250μA;

Figure 6: Drain-source breakdown voltage



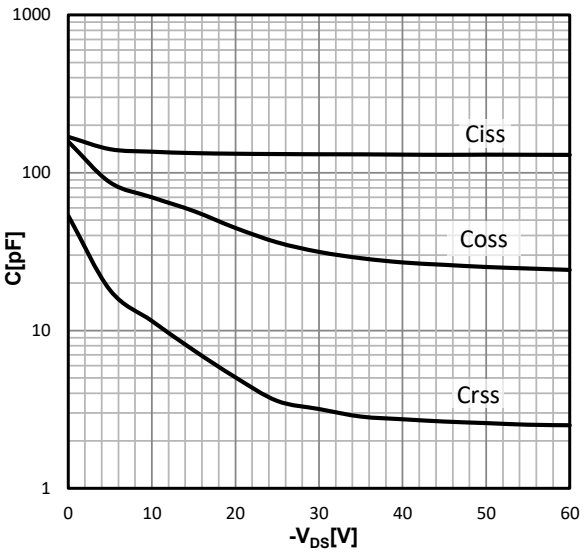
$V_{BR(DSS)}=f(T_j)$; I_D=-250μA;

Figure 7: Typ. gate charge



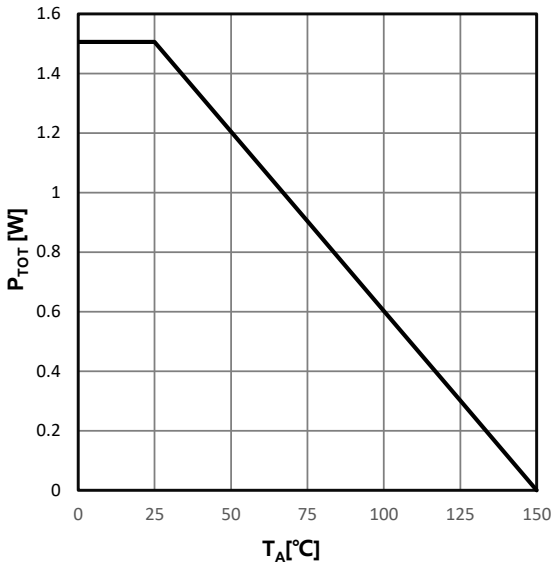
$V_{GS}=f(Q_g)$, I_D=-2.0A, T_j=25 °C; parameter: V_{DS}

Figure 8: Typ. Capacitances



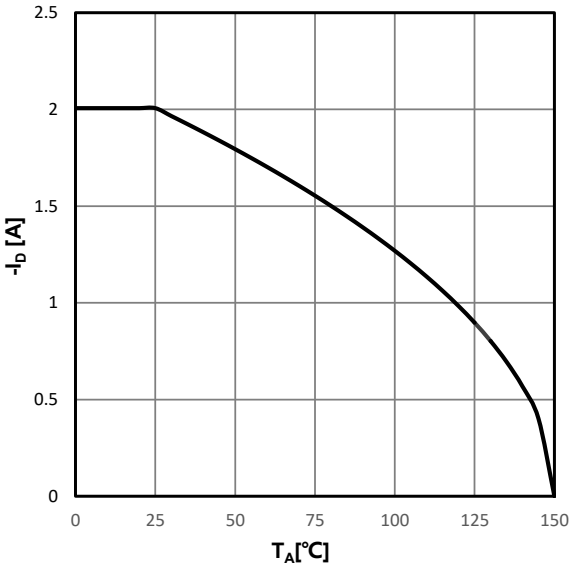
$C=f(V_{DS})$; V_{GS}=0V; f=1.0 MHz;

Figure 9: Power dissipation



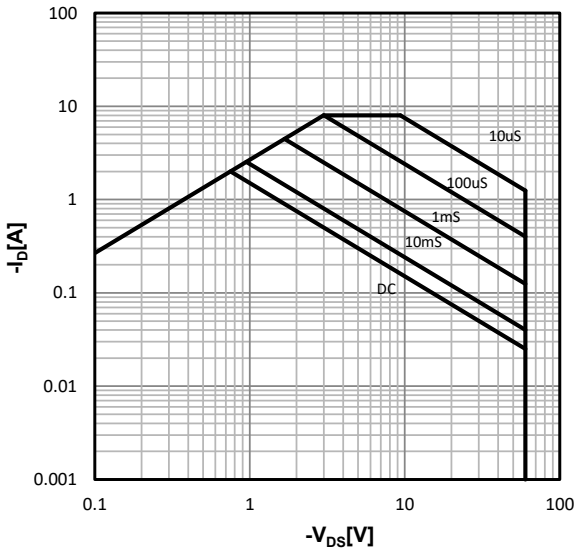
$P_{tot}=f(T_A)$;

Figure 10:Drain current



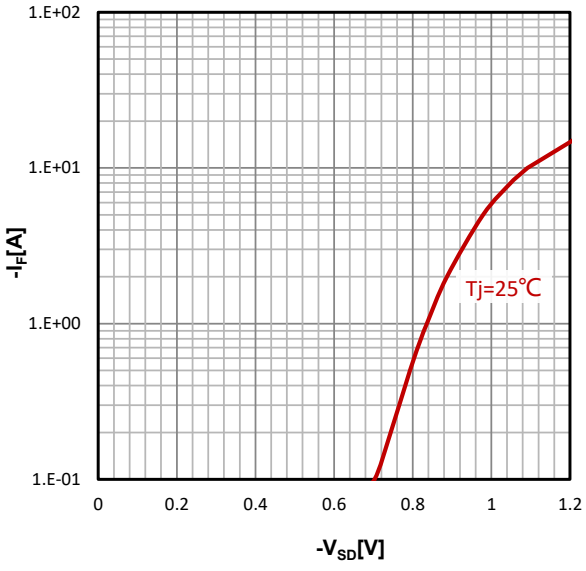
$I_D=f(T_A)$;

Figure 11: Safe operating area



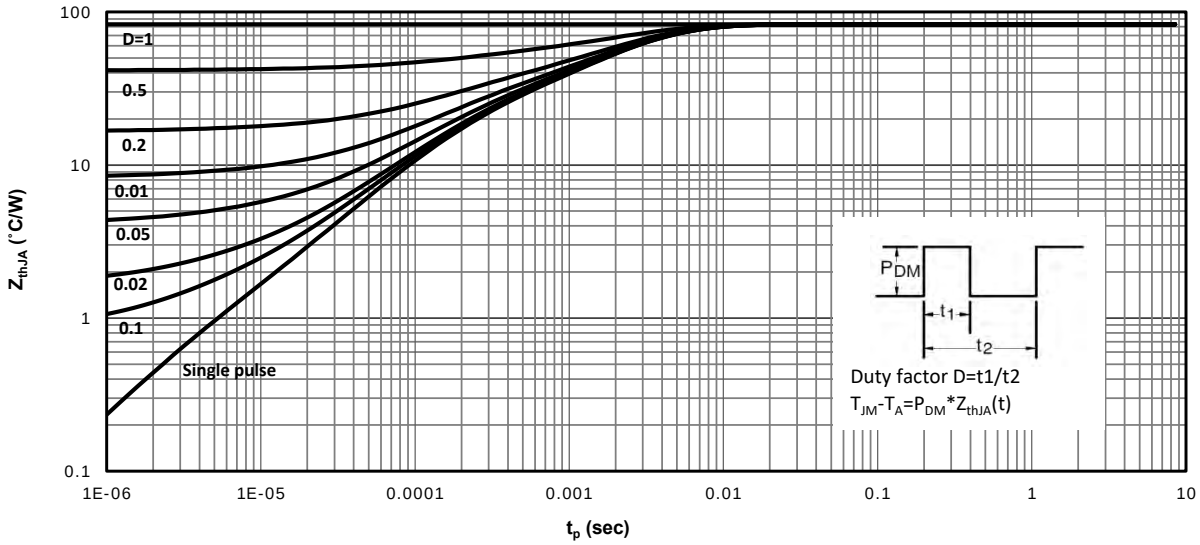
$I_D=f(V_{DS})$; $T_A=25$ °C; D=0; parameter: tp

Figure 12: Typ. forward characteristics



$I_F=f(V_{SD})$;

Figure 13: Max. Transient Thermal Impedance



$Z_{thJA}=f(t_p)$; parameter: D

Test Circuit & Waveform

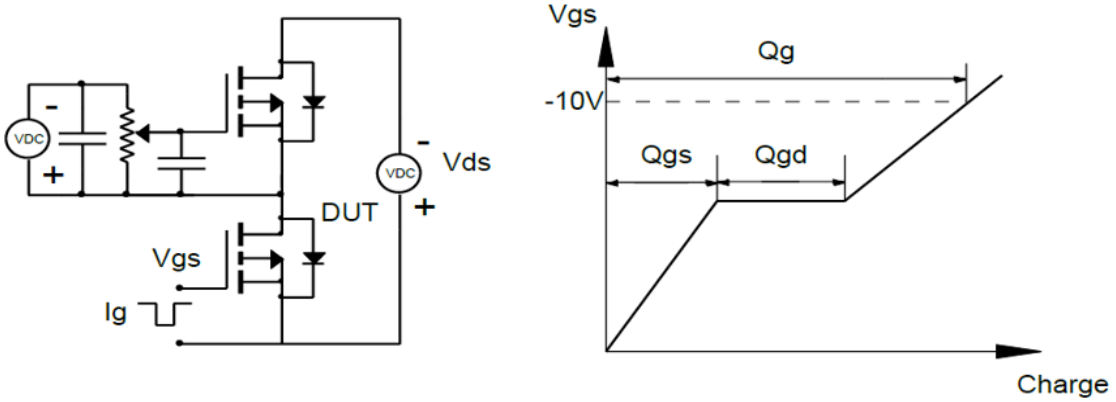


Figure 14: Gate Charge Test Circuit & Waveform

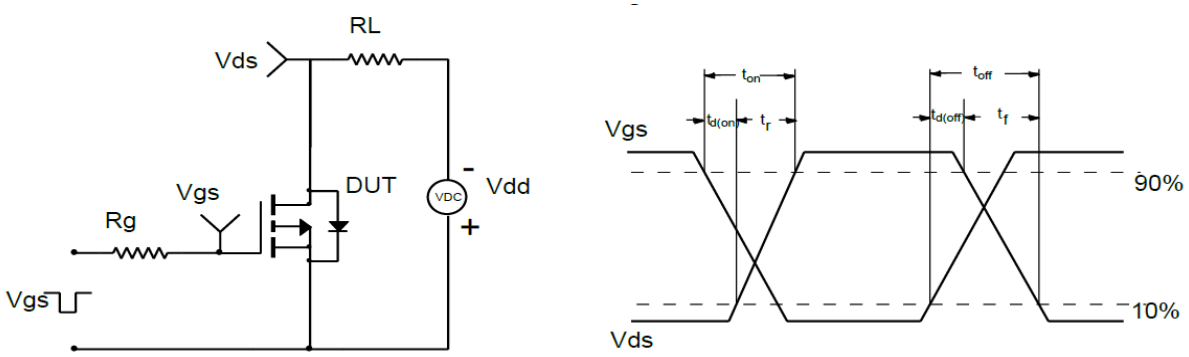


Figure 15: Resistive Switching Test Circuit & Waveforms

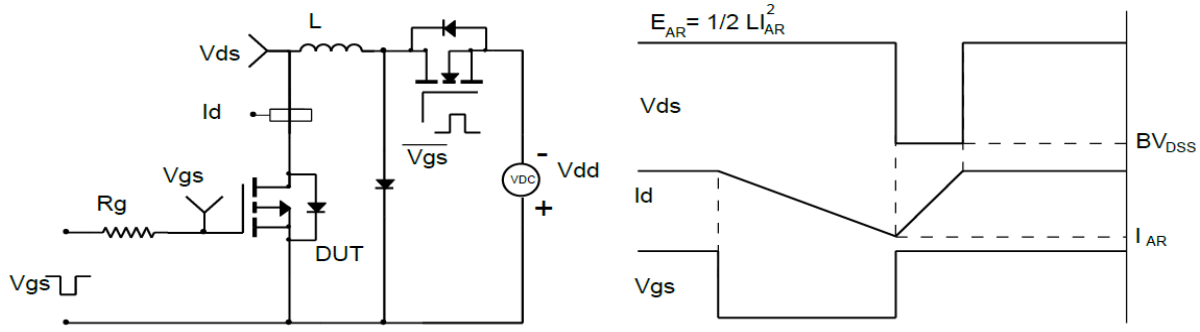
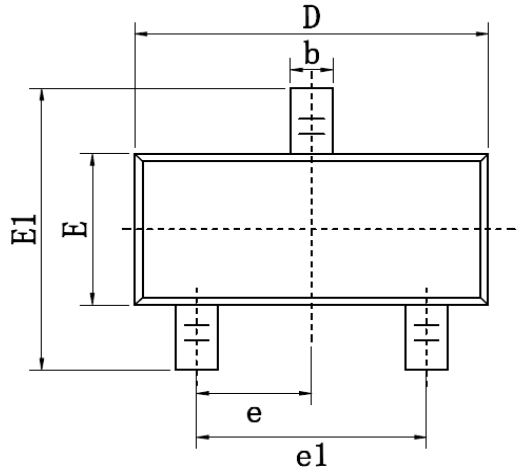
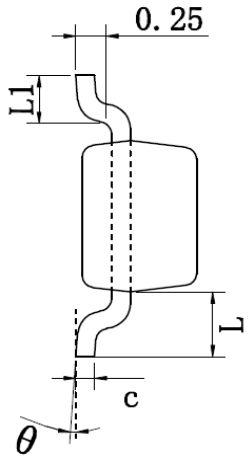
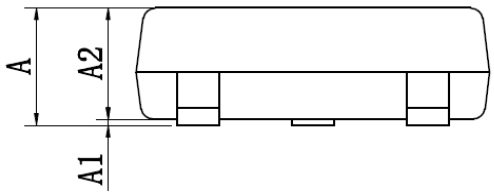


Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline







COMMON IN DIMENSION (MM)			
Symbol	**Min.**	**Nom.**	**Max.**
A	—	—	1.150
A1	0.000	—	0.100
A2	0.900	0.950	1.050
b	0.300	0.400	0.500
c	0.100	0.150	0.200
D	2.800	2.900	3.000
E	1.200	1.300	1.400
E1	2.250	2.400	2.550
e	0.950 TYP		
e1	1.800	1.900	2.000
L	0.550 REF		
L1	0.290	—	0.500

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Shanghai Leiditech Electronic Technology Co., Ltd.
Email: sale1@leiditech.com
Tel : +86- 021 50828806
Fax : +86- 021 50477059